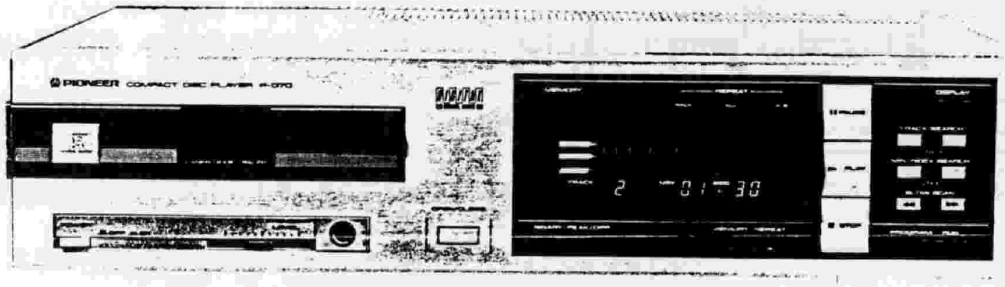
Technical Information

COMPACT DISC PLAYER

P-D70



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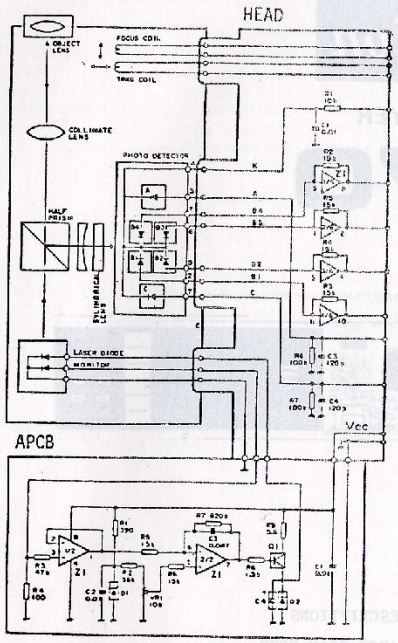
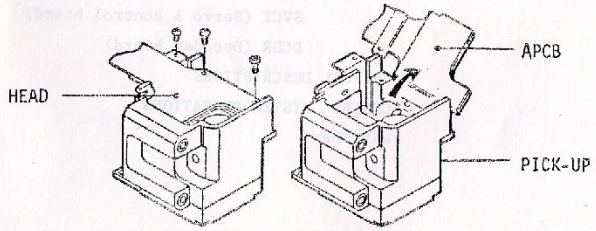
CIRCUIT DESCRIPTIONS



HEAD & APCB CIRCUIT



APCB

Although the LD optical output is dependent on the drive current, changes in the optical output can be generated by

temperature changes even when the current remains constant. To ensure that disc information is read correctly, light is beamed into pits in the surface of the disc and must be converted into a diffracted light intensity distribution. This necessitates holding the optical output at a constant level irrespective of changes in temperature.

The APCB contains the APC (Auto Power Control) circuit for automatic control of the optical output.

When the +Vcc is first started by the slow starter circuit on the PREB, a reference voltage of 3.3V is established by D1. This voltage is passed via VR1 and is applied to the non-inverted pin of Z1(2/2) where it is compared with the Z1(1/2) output. After being amplified by Z1(2/2) and current amplified by Q1, the voltage is used to drive the LD. C3 and R7 determine the frequency response when the APC is an open loop. The LD drive current from Q1 is converted to a laser beam output at a certain efficiency, and part of the optical output is received by MD where it is converted into a current. This MD output is passed via the Z1(1/2) buffer to the inverted input of Z1(2/2) to become the APC circuit loop error input. This ensures that the LD optical output is kept at a constant value.

The optical output can be adjusted by VR1 to obtain an

output emission of 0.26mW from the object lens.
Surge currents which can readily effect or damage the LD are blocked by D2 and C4.

HEAD

The HEAD board contains the circuit which converts the PD output (which is a very small current) to a voltage. The RF and focussing system has been set to obtain a DC output of 2.4Vtyp when bias resistances R2 thru R5 are applied to inverter Z1 (1/6 thru 4/6). The signal is also switched to low impedance by this circuit.
Because of board miniaturization and adjustment simplification, the tracking system receives the signal at R6 and R7 where it is converted to a voltage signal. C3 and C4 are used to limit the tracking system frequency band (fc = 26.5kHz approx).

PREB

The PREB board contains the circuit for executing arithmetic operations to obtain the RF signal, FCS error, and TRKG error signals from PD output signals converted to voltage signals on the HEAD board, plus the slow starter

circuit which supplies power to the APC circuit.
The focussing system signals RF, FOCS FIX, FOCS VAR, and FOCS SUM are generated from PD1, PD2, PD5, and PD6.

RF = PD1 + PD2 + PD5 + PD6 ------ (1)

FOCS FIX = PD1 - PD2 + PD5 - PD6 ------ (2)

FOCS VAR = Ditto

FOCS SUM = PD1 + PD2 + PD5 + PD6 ------ (3)

(Where PD1 thru PD7 are HEAD board outputs)

Operation (1) is executed by the RF amplifier consisting of transistors Q1 thru Q6, the resultant RF signal being passed to the DCDR board. Each PD signal is amplified some 6.4 times by this amplifier, and is adjusted to 0.5Vp-p AC by VR1 before being sent to the DCDR board as the RF signal. The band width is at least 10MHz, and the lower limit is set to about 500Hz by C5 thru C8.
Operation (2) is executed by Z1(1/2)(2/2) and Z2(1/2) to obtain the FOCS FIX and FOCS VAR signals. The band width in this case is set to about 28.4kHz by C14 thru C17, the signal being amplified by about 16 times. The signal amplified 16 times is passed to SVCT as the FOCS FIX signal used in controlling the focus servo loop. And the signal obtained by adjusting the gain of this FOCS FIX signal by VR3 is the FOCS VAR signal which is passed to SVCT as the focus servo error signal. VR2 is used to

adjust the offset for the two focus servo system signals, the control being adjusted to obtain the largest possible RF waveform "eye".

The FOCS SUM signal obtained by executing operation (3) in Z2(2/2) (gain of 47 times) is passed to SVCT where it is compared to determine whether the beam is "on track" or between tracks. High frequency components are removed from this signal.

The tracking system signals PD3 and PD7 are amplified 11 times by Z3(1/2)(2/2) to obtain the TRKG VAR and TRKG SUM signals.

TRKG VAR = PD3' - PD7' ------- (4)

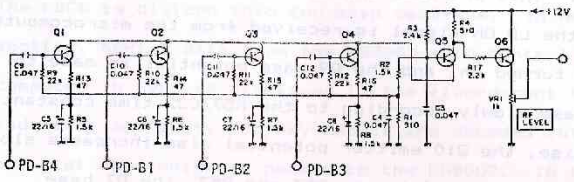
TRKG SUM = PD3' + PD7' ------- (5)

(Where PD3' and PD7' are Z3 outputs)

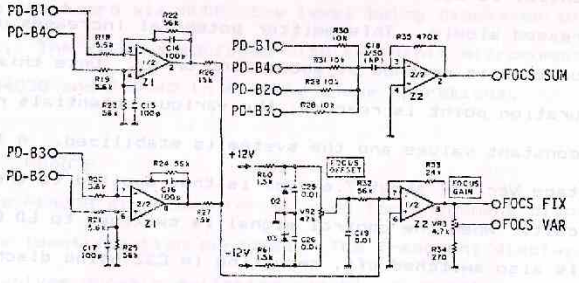
After operation (4) is executed by Z4(1/2) (gain of 4 times) and the tracking servo loop gain is adjusted by VR51, the TRKG VAR signal is set to about 2Vp-p when the loop is open. This signal is passed to the SVCT board where it is used as a tracking servo error signal. VR4 is used to adjust the balance of the tracking servo error signal, and the error signal is adjusted to be about 0V DC when the loop is open.

The TRKG SUM signal is generated by executing operation (5) by Z4(2/2) (gain of 1.5 times). This signal is also

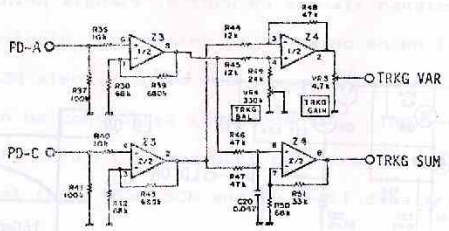
passed to the SVCT board where it is used as the DISC SENSE signal. C20 is used to limit the band width (to about 70Hz).



(A) RF



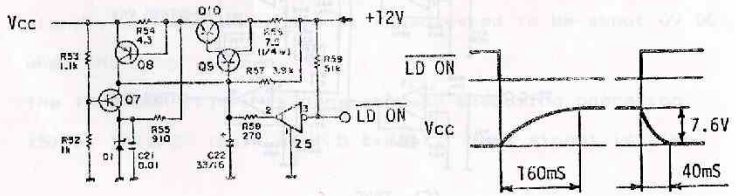
(B) FOCS



(C) TRKG

The slow starter circuit ensures that the APC power supply Vcc is given slow rise and fall times by means of an LD ON/OFF control signal from the microcomputer on the SVCT board. This protects the LD from surge currents.

When the LD ON signal is received from the microcomputer, Z5 is turned on, and the Q9 base potential is made to increase slowly according to the R57/C22 time constant. Likewise, the Q10 emitter potential also increases slowly, and following division by R53 and R57, the Q7 base potential is determined and the Q7 emitter potential is increased slowly. This emitter potential increases until saturation is reached at about 3.0V on D1. Once this saturation point is reached, the various potentials remain at constant values and the system is stabilized. A fixed voltage Vcc (of about 7.6Vtyp) is thus applied to the APC circuit. When the control signal is switched to LD OFF, Z5 is also switched off, resulting in C22 being discharged at a rate determined by the C22/R58 time constant. The various potentials consequently decrease until Vcc reaches 0V.



KDCB (Keyboard & Display Control Board)

1. Outline

The KDCB is divided into two main sections. In one section, serial data from the PD3007 main control microcomputer in SVCT is displayed in the fluorescent tube (FL) indicator and LEDs, and key inputs are decoded into 5-bit parallel data which is passed to the PD3007. In the other section, digital audio signals decoded by DASP are applied to the board via AUDF, the level being displayed in the FL. The KDCB is equipped with two 4-bit microcomputers PD4038 and PD4042 to execute these operations.

2. PD4038

The PD4038 microcomputer is used for 7-segment display and key identification purposes. The 7-segment display involves dynamic switching capable of handling displays of up to 8 digits. The dynamic switching data a thru h and the scanning signals 1G thru 8G are all handled in negative logic, the timing chart being shown in Fig.1. The PD4038 also includes four output ports P0 thru P3 which can be controlled independently. The 7-segment data and the P0 thru P3 output port data inputs are applied to the serial input pins SCK and SD. All data transfers are

completed in three serial transmissions where 16 bits form a single transmission unit. During this data transfer, a status output consisting of two bits SRS0 and SRS1 is sent to the sending side in response to each 16-bit transmission. The corresponding timing chart is shown in Fig.2.

The PD4038 also uses the dynamic switching scanning signals for key scanning purposes. By inverting the scanning signals and applying them to the key input pins KR0 thru KR3, an 8x4 matrix (maximum of 32 key inputs) can be covered. These key inputs are decoded into 5-bit codes for the key output pins KD0 thru KD4, and the key strobe pin KS is switched to low level while a key is being depressed. The key corresponding to the "11111" code, has been allocated for use in PD4038 self-testing mode.

3. Data Display and Key Input

The display elements on the KDCB include the 7-segment data display and level meter FL sections plus six LEDs (PLAY, PAUSE, MEMORY, TRACK, ALL, and A-B). The FL data display section and four of the LEDs (MEMORY, TRACK, ALL, and A-B) are switched by the PD4038. The PLAY and PAUSE LEDs are switched directly by PD3007. The FL grid arrangement is shown in Fig.3, the segment arrangement is

shown in Fig.4, and a table indicating the internal connections for each segment is given in Fig.5. This system requires a voltage to heat the filaments when the FL is switched on, a voltage to activate to the grid segments, and a cut-off bias to ensure that the display is properly turned off. The basic FL drive circuit and the relevant potential levels are shown in Fig.6.

The KDCB is equipped with 16 switches, 15 of them being located in the PD4038 key matrix. Fig.7 outlines a part of the key circuit when the PLAY switch depressed. For the PD4038 to detect that the PLAY switch has been depressed, the 4G scan signal is inverted and applied to the KR0 key input pin. And since the PAUSE switch and other switches are connected to the same key input pin, there is risk of two scanning signal output pins being short-circuited if two separate switches are pressed at the same time. D1 thru D5 have been inserted to avoid this situation. If a scanning signal is switched to low level when a switch is switched on, however, the D1 anode will not become exactly 0V due to the forward voltage applied to the diodes. Since this situation can prevent proper operation of the inverter, diodes D6 thru D9 have also been inserted.

4. PD4042 and Level Meter

The PD4042 microcomputer is used to show the input level of input digital audio signals. The three display modes are (1) binary mode where 2's type 16-bit digital audio signals are converted to absolute values and the 12 upper order bits apart from the MSB are displayed, (2) normal bar graph type peak mode, and (3) off mode where the entire level meter display is cleared. The data, clock, and RL signals required by the PD4042 are applied to the SD, SCK, and L/R input pins. Note, however, that the R and L channel data is processed by the PD4042 on a time-sharing basis. Inputs can be controlled by gate circuit by using the RCK and LCK pins which select the R channel or L channel clocks according to the need for data input. R and L channel data processed by PD4042 appears as 12-bit data outputs at the R1 thru R12 and L1 thru L12 output pins. This data is all negative logic. When the microcomputer is reset, binary mode is always selected. This mode is then switched to peak mode and off mode in that order whenever a KEY input is applied.

5. Miscellaneous

The PD4038 and PD4042 clock is obtained from a ceramic resonator which is oscillated by PD4042 and supplied to

PD4038. The reset pins, too, are connected in common and are reset by PD3007.

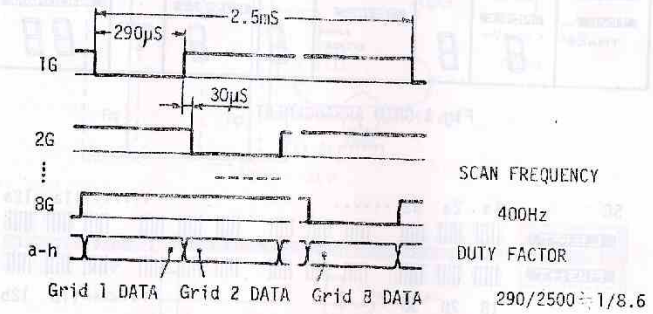


Fig.1 Display timing chart

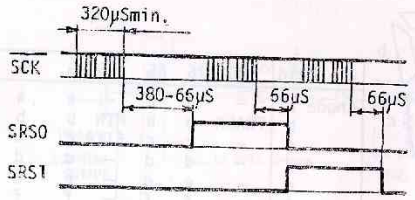


Fig.2 Transmission timing chart

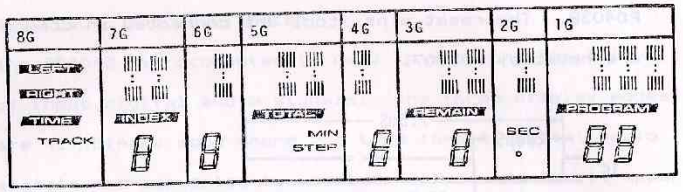


Fig.3 GRID ARRANGEMENT

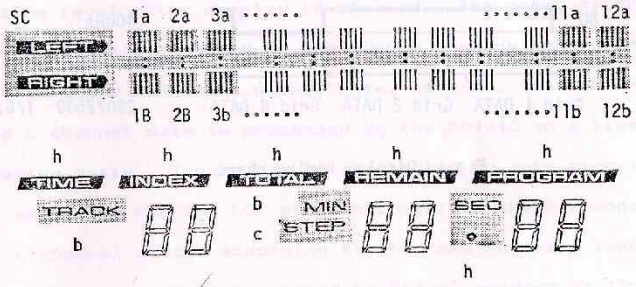
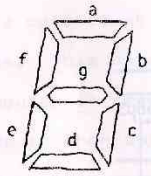
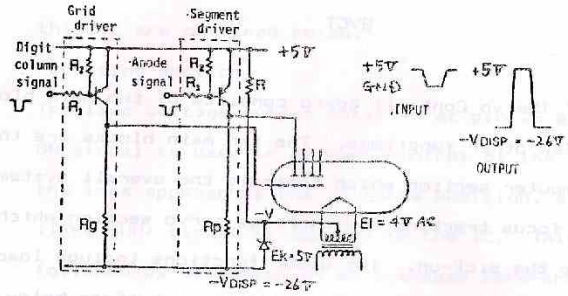


Fig. 4 SEGMENT ARRANGEMENT



Grid		8G	7G	6G	5G	4G	3G	2G	1G
Anode	a	—	a	a	—	a	a	a	a
	b	TRACK	b	b	MIN	b	b	b	b
	c	—	c	c	STEP	c	c	c	c
	d	—	d	d	—	d	d	d	d
	e	—	e	e	—	e	e	e	e
	f	—	f	f	—	f	f	f	f
	g	—	g	g	—	g	g	g	g
	h	TIME	INDEX	—	TOTAL	—	REMAIN	SEC	PROGRAM

Fig. 5 INTERNAL CONNECTION TABLE



FL Drive waveform

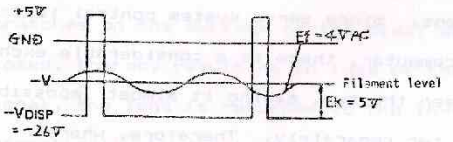


Fig.6 FL drive circuit

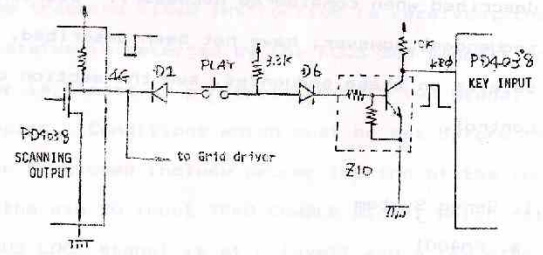


Fig.7 Key circuit

SVCT

The SVCT (Servo Control) board consists of two main blocks plus a few other functions. The two main blocks are the microcomputer section which controls the overall system, and the focus tracking and carriage servo section which controls the pick-up. The other functions include loading motor drive. A description of the servo systems below is followed by a description of the microcomputer, plus the other functions. Since servo system control is executed by the microcomputer, there is a considerable exchange of signals between the two, making it almost impossible to consider the two separately. Therefore, where microcomputer control signals are referred to in the following servo system description, those signals are also described when considered necessary. Starting and search sequences, however, have not been described. For further details on these sequences, see the section on system control.

1. Servo System

a. PM4001

This IC has been developed by Pioneer for use in the focus, tracking, and carriage servos. The functions of

this IC are outlined below.

Focussing section

The lamp voltage output obtained at pin 28 by the FOCUS ON signal is used in up/down control of the lens. When the lens approaches the in-focus position, a DISC SENSE (TRKG SUM) signal is applied to the IC. This is followed by detection of an S-shaped zero-cross by a FOCS FIX signal, and loop closure by pin 25. If the lens is put out of focus (by strong shock or large scratches on the surface of the disc) while the loop is closed, thereby resulting in loss of the DISC SENSE signal, the lens is returned to the in-focus position automatically by first being temporarily lowered for recommencement of the focussing operation.

Tracking section

When the tracking close instruction is received, the "on track" status is detected by the FOCS SUM signal; and the loop is closed by pin 4 at the TRKG VAR signal zero-cross point. Conditions which must be met before the loop can be closed include proper locking of the focus (where the pin 20 input TRKG ENABLE signal which delayed the FOCUS LOCK signal is at L level) and a tracking error frequency lower than the frequency set by pins 10 and 11. If the output which integrated the tracking

return voltage is applied to pin 6, and an abnormal DC current is consequently passed through the tracking actuator, that current is detected, a stopper is activated, and the loop is forced open for a certain period of time as determined by pins 7 and 8. And if a jump instruction is received, the loop is opened immediately and a jump pulse output is generated from pin 5. The differentiated version of this signal is then applied to the actuator. When the loop is closed again at the tracking error zero-cross point (exactly midway between adjacent tracks), the pin 5 jump pulse is switched off at the same time, resulting in the pulse being differentiated and applied to the actuator as a control pulse. The jump pulse polarity is switched by the FWD/REV instruction, resulting in smoothly executed jump forward and jump back operations.

Carriage section

An output voltage of ±4V is generated on pin 13 by the SCAN instruction and the FWD/REV signal, and is applied to the carriage motor to commence scanning operation. When the tracking servo is closed, the CARG O/C signal on pin 12 is changed to -5V resulting in closure of the carriage loop. Hence, since the carriage is always moved by low frequency components of the tracking

actuator current, the ideal actuator is centered about a neutral position without offset to enable tracing of eccentric paths.

An internal block diagram of the PM4001 is given in Fig.1 below.

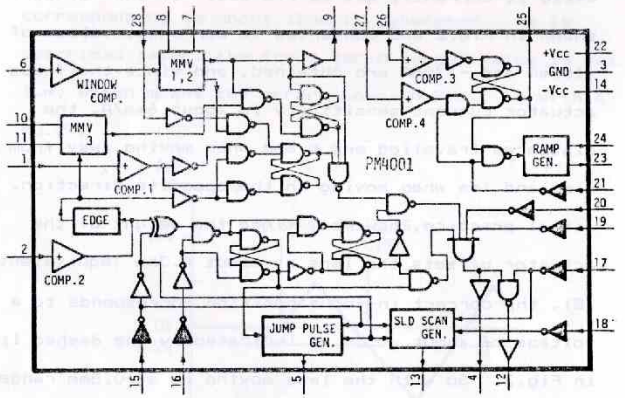


Fig.1 PM4001 internal block diagram

b. Focus servo system

When the FOCS ON signal from the microcomputer is applied to pin 21, a LENS UP/DOWN signal is generated from pin 24. The frequency (lens up speed) of this signal is determined by C4 connected externally to pin 24, and the subsequent focus actuator drive current waveform is shown in Fig.2 below. A single UP/DOWN cycle is currently set to 0.8 sec. If the voltages shown in Fig.2 are converted to currents, values of +100mA and -170mA are obtained, and since the focus actuator current sensitivity is about 6mm/A, the distances travelled are 0.6mm when moving away from the disc and 1mm when moving in the opposite direction. In actual practice, however, since the weight of the actuator offsets the lens by about 0.3mm (equivalent to 1G), the correct in-focus position corresponds to a voltage of about -0.2V as indicated by the dashed line in Fig.2. So with the lens moving in a +0.8mm range centered about the focus point, it must always move through the correct focus point.

When the lens comes close to the focus point, the TRKG SUM signal (TRKG A+B) is applied to pin 27 of the IC where it is used as the DISC SENSE signal. A disc is judged to be present when the level at an internal

comparator exceeds +0.6V. When the lens is in focus, a DC voltage of about 3V is maintained, and is passed though a LPF on the pre-board to ensure that the voltage does not drop below 0.6V when a scratch is encountered on the disc.

When the lens is moved up and down (see Fig.2) the FOCS FIX signal (S-shaped error shown in Fig.3) is applied to pin 26. In normal discs, an error of about 3Vp-p corresponding to about 15um is generated. As is described later, the focus servo target value is set to 1um, which means the error shown in Fig.3 is within ±0.2V.

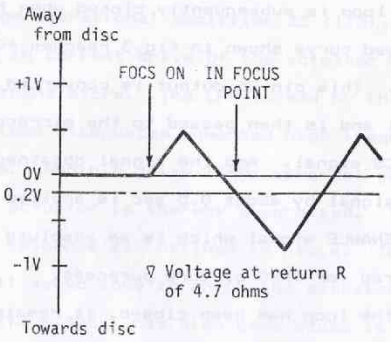


Fig.2 FOCS drive current during lens up/down operations

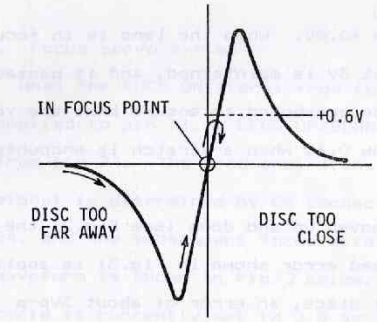


Fig.3 S-shaped FOCS error

Since the pin 26 comparator threshold has been set to +0.6V, the pin 25 output is switched to -5V and the focus loop is subsequently closed when the level of the S-shaped curve shown in Fig.3 reaches +0.6V (the dashed line). This pin 25 output is converted to a TTL level signal and is then passed to the microcomputer as the IN FOCS signal. And the signal obtained by delaying this signal by about 0.5 sec is applied to pin 20 as the TRKG ENABLE signal which is an absolute precondition required for TRKG closure purposes.

Once the loop has been closed, it remains closed as long as the microcomputer does not switch the FOCS ON signal to H level. If, however, a serious scratch is encountered on the disc surface, or a strong external

shock is received, the lens may be thrown out of focus. Since the DISC SENSE signal is stopped in this case, the loop is opened, and the "lens up" operation is repeated from the beginning again to refocus the lens.

The FOCS VAR signal which is gain adjusted (level attenuation) on the pre-board is applied to Z1(1/2) which includes an equalizer circuit where phase advance is compensated in the R1, R2, C1 stage and phase delay is compensated in the R3, C2 stage. In addition, the FET Q1 loop switch is included in the feedback loop, and closure timing is controlled by pin 25 of the above IC.

The phase compensated FOCS VAR signal is passed to the final stage operational amplifier Z2 (1/2), thereby resulting in current drive of the actuator by the Q2 and Q3 drive transistors. The LPF formed by the R11/C5 feedback loop attenuates unwanted high frequency components. Audible noise (3kHz upwards) generated by the focus actuator is thereby suppressed. The equalizer frequency response is outlined in Fig.4. The gain of the overall servo zone to which the actuator frequency response (fo = 30Hz) has also been added is set to 650Hz 0dB for open loop (and to 700Hz 90° for closed loop) so that the level for the target value of 1um does not drop below the disc specifications.

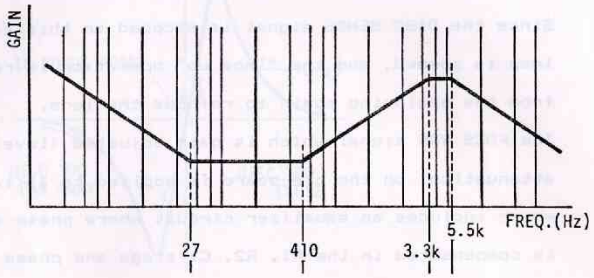
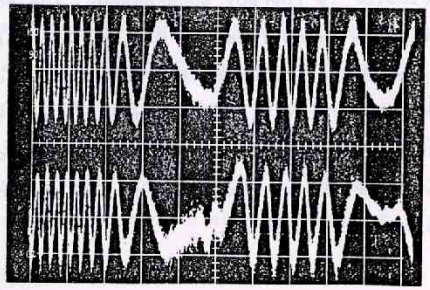


Fig. 4 FOCS equalizer gain frequency response

c. Tracking servo

The TRKG VAR signal generated on the pre-board and level adjusted by gain control is passed to pin 2 of the IC and to the source of the Q12 loop switch. The waveform existent while the tracking loop is open is shown in Fig.5. An error of about 2Vp-p is generated with ordinary discs.



Top: TRKG VAR
1V/div

Bottom: FOCS SUM
1V/div

H: 5ms/div

Fig.5 TRKG VAR
& FOCS SUM

The error shown in Fig.5 is set to 0V by either having the beam exactly "on track", or halfway between adjacent tracks. To decide which case applies, the FOCS SUM signal (the sum signal of four separate parts) is applied to pin 1 of the IC. This pin is connected internally to a comparator with a threshold level of 0V. Pin 2 of this IC is also connected internally to a 0V threshold comparator, and it is to this pin that the previous TRKG VAR signal is applied. The correct "on track" status is detected from these two signals according to the logic shown in Fig.6. This is where the tracking servo loop is closed.

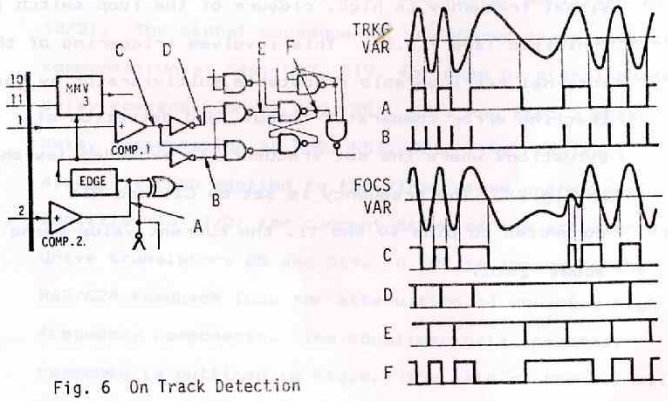


Fig. 6 On Track Detection

The "on track" status is detected by the above logic when the TRKG O/C signal from the microcomputer is at L level. And although a +4V output appears at pin 4 resulting in closure of the tracking loop, an absolute precondition for this is that the TRKG ENABLE signal described above under the focus servo section must be at L level (that is, focus must be securely locked). In other words, if the lens is put out of focus for any reason during playback (where the tracking loop is closed), the tracking loop is opened immediately.
To simplify the lock-in operation, use is made of the frequency detector logic. That is, if the TRKG VAR signal frequency is high, closure of the loop switch is inhibited (see Fig.5). This involves triggering of the internal retriggerable monostable multivibrator by the tracking error comparator output, and detection of situations where the set frequency is exceeded (as shown in Fig.7). The frequency is set by C16 and R36 connected to pins 10 and 11, the current value being about 2 kHz.

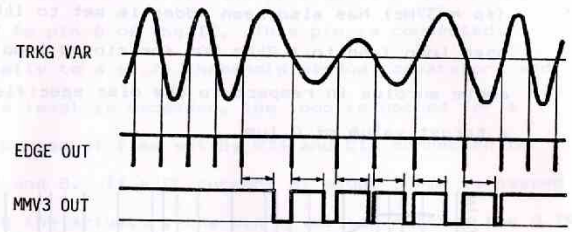


Fig. 7 TRKG VAR frequency detection

The TRKG VAR signal is applied to the Q12 FET switch (where the gate potential is controlled from pin 4 according to the timing described above), and then to an equalizer amplifier Z1(2/2) and buffer amplifier Z2 (2/2). The signal subsequently undergoes phase advance compensation at R46, R47, C19, followed by step 1 phase delay compensation at R50, R51, C20, and step 2 phase delay compensation at R52, R53, C21. The resultant signal is then applied to the final stage operational amplifier Z6 (1/2) for current drive of the actuator by drive transistors Q5 and Q19. A LPF is formed by the R63/C24 feedback loop for attenuation of unwanted high frequency components. The equalizer gain frequency response is outlined in Fig.8. The gain of the overall servo zone to which the actuator frequency response

(fo = 37Hz) has also been added is set to 1kHz 0dB for open loop (and to 1.2kHz 90° for closed loop) to ensure ample surplus in respect to the disc specifications with a target value of 0.1um.

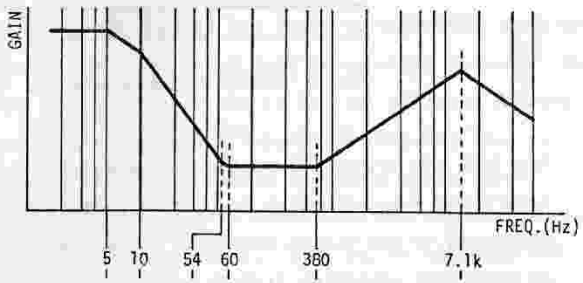


Fig.8 TRKG equalizer gain frequency response

The next item to be described in the actuator stopper. If an excessively large DC current is passed through the actuator as a result of an abnormal condition arising in the circuitry or optical system, or if a disc with serious eccentricity problems is loaded, the actuator is in danger of burning out due to the additional heat generated. The actuator stopper is used to avoid this situation. The voltage across the actuator return resistance (R72: 2.7-ohm) is integrated (1Hz cut-off)

and applied to Z7 (1/2), the subsequent output being passed to pin 6 of the IC. This pin is connected internally to a ±0.7V threshold window comparator, and if this level is exceeded, the loop is opened for a fixed period of time set by R34 and C15 connected to pins 7 and 8. If a DC current of about 300mA is passed through the actuator, the pin 6 voltage reaches the 0.7V level, and the loop is opened for about 10msec and pin 9 is switched to L level during this interval. Since this 10msec interval (the limit for the IC internal monostable multivibrator) is not sufficient to adequately protect the actuator, Z5 (monostable multivibrator) is triggered by the pin 9 output, resulting in the loop switch control pin (pin 4) being forcibly switched to -5V by Q13 and Q14 for about one second, thereby keeping the loop open for that period. Since 300mA corresponds to about 0.3mm, and has been set to be more or less the same as the movable range (angle of vision) of the tracking actuator, there is little likelihood of the stopper being operated by mistake.

Waveforms at different positions when a JUMP FWD is executed are shown in Fig.9. First the JUMP TRIG instruction from the microcomputer is applied to pin 16, the direction being applied to pin 15 by the FWD/REV

signal. At the trailing edge of the JUMP TRIG signal, the loop switch is opened immediately, and at the same time a jump pulse output apears at pin 5. This output is differentiated, and the pulse where the wave height is limited by Q15 and Q16 is passed via R62 to Z6(1/2) for application to the actuator. When the beam subsequently reaches a point midway between tracks where the error is 0V, this fact is detected by the pin 2 comparator, resulting in the loop being closed at the same time that the pin 5 jump pulse is switched off. Then as a result of subsequent differentiation, a damping pulse of opposite polarity to the pervious pulse is generated and a brake action is applied. Hence, the tracking error is controlled to enable stable jumping to be executed. The JUMP REV operation is almost exactly the same, the jump pulse output on pin 5 in this case being -5V. The polarity of the differentiation waveform is again reversed. When consecutive track jumping is executed as during search mode. JUMP TRIG input signals are applied at 7msec intervals. But as can be seen from the time axis in Fig.9, a single jump is completed within about 800usec, thereby enabling smooth multiple jump operations to be executed.

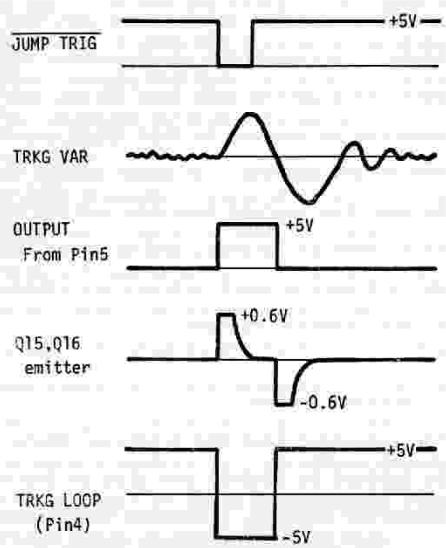


Fig. 9 Jump operation waveforms
(Jump forward)

VR1 is the tracking offset adjustment control used to absorb circuit offset on the SVCT board. The voltage across the tracking return resistance (R72) when the

power is switched on is adjusted to 0V by this control. The FOCS SUM signal is applied to the Z4 comparator (+0.3V threshold) where it becomes the track count signal. Although the microcomputer scans the carriage with the tracking loop open during search operations, scanning is stopped by this track count signal when near the target address. In other words, the difference between the current position and the target address is calculated in advance, and scanning proceeds while the above tracking count signals are received one at a time by the internal counter.

d. Carriage system

The voltage across the tracking return resistance (R72) is applied to Z7(2/2) and also to the final stage amplifier Z6(2/2), resulting in voltage drive of the carriage motor by the drive transistors Q6 and Q7. The Z7(2/2) equalizer amplifier must satisfy the following two requirements. (1) When there is little eccentricity, the zone has to be expanded to improve the carriage motor response. And (2) when there is considerable eccentricity, on the other hand, the zone has to be narrowed and the gain in the eccentricity range (3 to 8Hz) has to be dropped because of the resultant

inconvenience generated by the larger phase difference between the amplifier and the tracking actuator when the carriage is complying with the greater eccentricity. To meet this requirement, the gain in this region is decreased for discs of considerable eccentricity by D11, D12, R76, and C28.

The Z7(2/2) gain frequency response is outlined in Fig.10. Since the DC gain is 25dB, and the carriage motor starting voltage about 1.5V, the carriage will comply with actuator changes of about 30um. The characteristics indicated by the full line in Fig.10 are obtained when there is little eccentricity, while the characteristics approach the dashed line when there is considerably more eccentricity. In actual practice, however, a "soft clip" by diode is employed, resulting in the carriage drive waveform shown in Fig.11. The base of the transistor switch Q17 included in the Z7(2/2) feedback loop is controlled by the CARG O/C signal from pin 12. The carriage loop is always closed whenever the tracking loop is closed, and also remains closed during jump operations.

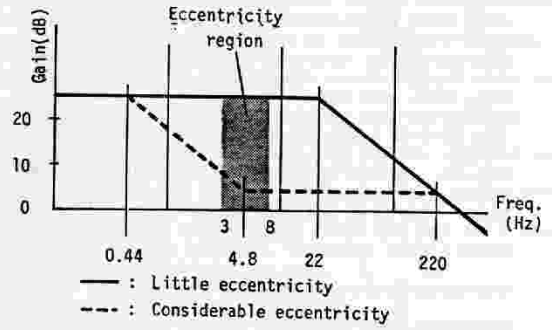


Fig.10 Z7(2/2) Gain frequency response

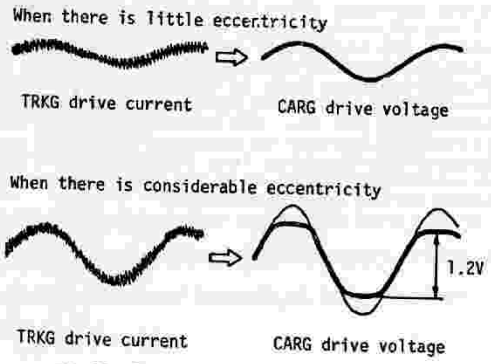


Fig.11 Eccentricity and CARG drive

When the carriage is moved, the SCAN signal applied to pin 17 from the microcomputer is switched to H level, direction is determined by the pin 15 FWD/REV signal, and a ±4V SCAN voltage is generated on pin 13. This signal is applied to the Z6(2/2) operational amplifier in the final stage, resulting in a -9V voltage being applied to the carriage motor during FWD SCAN, and a +9V voltage being applied during REV SCAN. The slider is thus moved from the inside edge to the outside edge in about three seconds.

2. Microcomputer Section

The SVCT microcomputer section includes an 8-bit microcomputer PD3007 (Hitachi 8-bit microcomputer HD6805V) and a data selector 74LS157. The PD3007 I/O ports are listed below (where encircled numbers denote input ports).

▽ A PORT

Pin no.	Pin name	Function
40	F/$\overline{R}$	fwd ⌋ rev
39	JUMP TRIG	trailing edge
38	SCAN	
37	SLOW/$\overline{FAST}$	slow ⌋ fast
36	TRKG	TRKG loop open ⌋ close
35	FOCS	FOCS loop open ⌋ close
㉞	$\overline{IN\ FOCUS}$	⌉FOCS locked
㉝	$\overline{RF}$	⌉RF detected

▽ B PORT

Pin no.	Pin name	Function
32	$\overline{MUTE}$	⌉Aud. muting
31	$\overline{ATT}$	⌉Aud. attenuating(-12dB)
30	$\overline{SPDL\ RUN}$	
29	QDRD *1	leading edge
㉘	$\overline{FSLOCK}$ *2	⌉locked
27	——	——
26	PLAY	
25	$\overline{PAUSE}$	

*1: Q Data ReaD strobe

*2: Frame Sync. LOCK

▽ C PORT

Pin 16 SD/QDAS

This port serves 3 separate pur poses: (1) serial data in communication with KDCB, (2) select signal when reading key data and status, and (3) data/flag select signal when reading sub-code data from DCDR.

Pin 15 $\overline{SCK}$ Serial ClocK

Pin 14 $\overline{RESET}$

PD4038 (and PD4042) is reset after the power is switched on, and when signals cannot be passed to PD4038.

Pin 13,12 LOAD B, LOAD A

LOAD A	LOAD B	Operation
L	L	stop
L	H	eject
H	L	load disc
H	H	—— *

*: Altough a short brake is applied when both LOAD A and LOAD B are set to "H", this mode is not used.

Pin ⑪ $\overline{CLMP}$

Set to "L" when the disc table is moved right in and the clamper lowered.

Pin ⑩ $\overline{DOOR}$

Set to "L" when the disc table is moved right out and the microswitch is pressed.

Pin⑨ $\overline{INSIDE}$

Set to "L" when the slider is returned to the home position.

▽ D PORT

Pin no.	When QDAS is "L"	When QDAS is "H"	
⑰	KD3	SRS 1	See the KDCB description.
⑱	KD2	SRS 0	
⑲	KD1	$\overline{K\text{-}S}$	
⑳	KD 0	KD4	
㉑	QDRE	QDAa	See the DCDR description.
㉒	QDEa	QDAb	
㉓	QDEb	QDAc	
㉔	("L")	QDAd	

▽ KEY MATRIX

Key	KD4	KD3	KD2	KD1	KD0	Key	KD4	KD3	KD2	KD1	KD0
PLAY	0	0	0	1	1	PLAY*	1	0	0	1	1
PAUSE	0	0	1	0	0	PAUSE*	1	0	1	0	0
TRACK REV	0	0	1	0	1	SLOW REV	1	0	1	0	1
TRACK FWD	0	0	1	1	0	SLOW FWD	1	0	1	1	0
OPEN/CLOSE	0	0	1	1	1	REPEAT	1	0	1	1	1
STOP	0	1	0	1	1	TRACK REV*	1	1	0	1	1
DISP	0	1	1	0	0	TRACK FWD*	1	1	1	0	0
MIN REV	0	1	1	0	1	PROGRAM	1	1	1	0	1
MIN FWD	0	1	1	1	0	RUN	1	1	1	1	0
MEMORY	0	1	1	1	1						

* marked keys are located on the remote control unit.

3. Other Functions (Loading Circuit)

Z9 is an IC used for forward and reverse drive of the motor by TTL control signals. The loading motor an a series resistance R88 (6.8-ohm) are connected between pins 2 and 6. When an H level signal from the microcomputer is applied to pin 3, pin 6 is switched to +12V and pin 2 to GND, resulting in the disc table be moved in. If an H level signal is applied to pin 5, on the other hand, pin 2 is switched to +12V and pin 6 to GND, and the disc table is moved out. Normally, pins 3 and 5 are at L level, and pins 2 and 6 are both open.

A protector circuit is used to detect any dangerous situation (such as a finger being caught while the disc table is being slid back into the set) and to subsequently stop the loading motor. During normal load-in operations, the current passed through the loading motor is about 100mA, resulting in a voltage of 0.68V being generated across both ends of the 6.8-ohm resistance. VR2 is used to adjust the voltage between TP6 and TP7 to 0.4V. If an abnormal condition arises and the load is increased, the counter electromotive voltage is reduced, resulting in an increase in the current. The Q9 transistor is

consequently turned on. Q10 is turned off, and pin 13 of Z10 is switched to L level. The flip-flop, therefore, is inverted and pin 11 of Z10 is also switched to L level. Pin 3 of Z10 is switched to H level at this time, resulting in Q11 being turned on and pin 3 of Z9 being forced to switch to L level. In this situation the loading operation is stopped.
The current is also increased when loading is first started, and this could be detected by mistake resulting in the operation being stopped again. This is avoided by turning Q10 on by a pulse signal obtained by integrating the leading edge at pin 3 of Z9 and passed via D5. And to prevent a similar occurrence as a result of the +12V laser diode power supply being applied if the disc table catches the rubber edge of the shaft when just about all the way in, the L level on pin 3 of Z10 is kept fixed at L level by switching pin 2 to H level by 12V applied to the +12V IN pin.

While the clamp switch is being depressed, Q8 is on and the disc lamp lights up.

DCDR

The DCDR board is divided into seven main blocks.

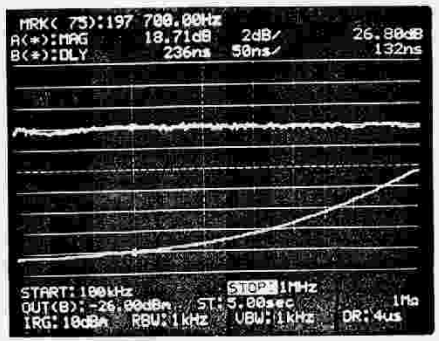
1. RF equalizer
2. ATC
3. RF detector
4. Clock sampling PLL
5. Sync and data separation
6. Error correction and jitter absorption
7. Disc drive

Due to the relationship between the pick-up spatial frequency characteristics and pit dimensions, the low frequency components of the RF signal detected by the pick-up and amplified by PREB are attenuated more than the high frequency components. Therefore, the amplitude characteristics are compensated by the RF equalizer with flat delay characteristics, thereby forming a signal which is easy to demodulate.
The EFM signal thus formed is then converted to TTL level by the ATC circuit. The RF detector circuit is employed for mirror surface detection and PLL OFF purposes. The EFM signal converted to TTL level (EFM2) is passed to the clock sampling PLL circuit which in conjunction with a VCO circuit samples PLCK signals. The EFM is activated by the leading edge of the PLCK signal, and the waveformed signal (EFM1) is passed together with the PLCK and EFM2 signals to the Sync and data separation LSI (TC9178F) where EFM demodulated, sub-code demodulated, and CLV control signals are sampled.
The demodulated data undergoes error correction and jitter absorption in a correction LSI & RAM before being passed to the AUDF together with clock and serial data.
Furthermore, frequency and phase servo control signals are generated by referrence clock and playback frame sync for disc drive at constant linearity.

1. RF EQUALIZER

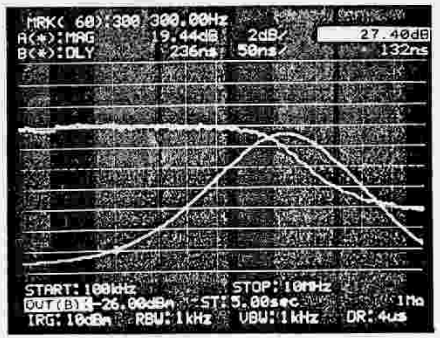
Because of the optical frequency characteristics, the high frequency components of the RF signal obtained by the pick-up are attenuated more than the low frequency components. The delay time, however remains constant. For this reason, compasation involves boosting of only the high frequency components at constant delay.

The high region increment phase delay circuit is formed bu Q1,C2,R4 and R5, while the high region increment phase advance circuit is formed by Q2, R6, R7, R8, and C4. This enables a 12dB/oct high region increment and flat delay RFEQ to be achieved.



Delay 50nS/div

Gain 2dB/div

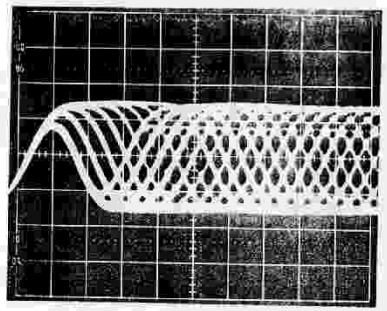


Delay 50nS/div

Gain 2dB/div

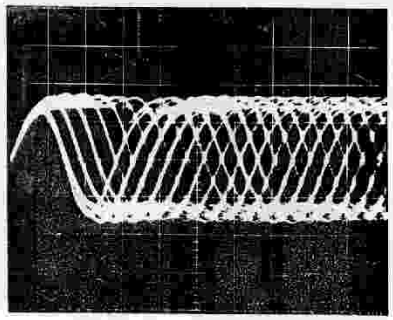
Since the RF signal played back from disc contains very few components above 1MHz, the region above 2.2MHz is attenuated by C3 and R6. The RF equalizer gain in the vicinity of 200kHz is about 14dB, and the RF level can be adjusted to 0.5Vp-p by the PREB VR1. Therefore, the RF signal standard level at the Q3 emitter is 2.5Vp-p.

The RF EQ input and output waveforms are shown below. Equalization enlarges the central diamond shapes (eye pattern) in the amplitude direction, thereby greatly improving the error factor after demodulation.



Before equalization

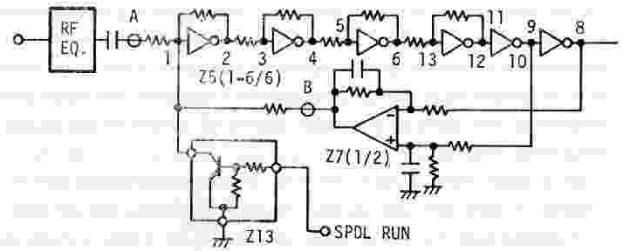
0.2V/div
0.5μS/div



After equalization

1.0V/div
0.5μS/div

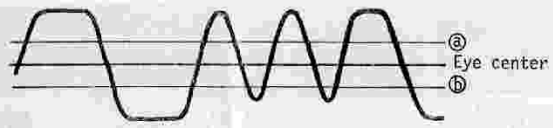
2. ATC Circuit



The EFM DSV (Digital Sum Value) is zero. That is, if the disc recording waveform is maintained flat for a long period of time, DC components are eliminated. This fact is one of the special features of this demodulation method.

The ATC circuit is used to set the optimum threshold level automatically during demodulation on the basis of this theory.

Since the C-MOS inverter is used as an operational AMP in this circuit, the threshold voltage may be considered as Vcc/2. Hence, feedback is applied to this circuit so that the EFM eye center corresponds with the threshold voltage.

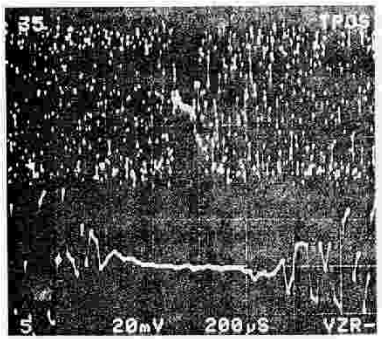


If the DC level of point A is assumed to be at level ⓐ in respect to the eye center of the EFM input, the H duration on pins 2,6 and 10, and the L duration on pins 4,12, and 8 is increased, resulting in point B becoming H. As a result, the EFM signal is "raised", and the eye center maintains equilibrium at the threshold voltage. Converselt, if the DC level of point A is assumed to be at level ⓑ, an L voltage is applied to point B, resulting in the EFM signal being "lowered", and the eye center maintaining equilibrium at the threshold voltage.

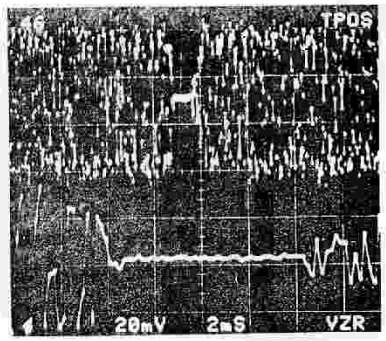
Since the actual EFM signal mainly contains spectrum components from the low frequency region (around several kHz), a better error factor can be expected if only low frequency components are handled. With scratched discs, however, overlapping with low fregencies caused by scratches will effect the RF waveform. And since CIRC error correction will no longer be possible, interpolation and previous value hold are generated, resulting in a certain amount of deterioration in the quality of sound.

To counteract this, a small ATC time constant is used to enable the control to cope with any changes during a drop-out. But setting the time constant at too low a value will result in a poorer error factor. The final value should be decided after also considering "playability" and the B.E.R. The EFM waveform in a defective disc is shown below with the ATC circuit both on and off.

And to prevent the ATC circuit from operating when the power is switched on, operation is inhibited by Z13. Z13 is enabled by $\overline{\text{INFOCUS}}$ to commence ATC operation.



$\overline{\text{ATC OFF}}$ Top: 2V/div, 2ms/div
Bottom: 2V/div, 200μs/div



$\overline{\text{ATC ON}}$ Top: 2V/div, 2ms/div
Bottom: 2V/div, 200μs/div

3. RF Detector Circuit

During search and rough feed, the microcomputer moves the carriage while counting the number of tracks up to the target address, calculating on the basis of data read from the TOC. During these operations, the beam spot may sometimes go beyond the lead-out track onto the mirror surface portion. And since the EFM signal is no longer generated if this happens, the spindle servo will proceed to a runaway situation. To avoid this condition, the microcomputer must be able to reverse the carriage direction and return it to the signal portion of the disc. For this reason, an RF detector circuit is used to detect whether the carriage is on the information area or the mirror surface portion, the detection result being sent to the SVCT board as the $\overline{\text{RF(SENS)}}$ signal ($\overline{\text{RF present}}$).

And to ensure that RF detection functions correctly without being effected by eccentricity and other similar factors, the microcomputer stops the carriage after allowing 5msec to elapse following reception of the "RF present" signal.

The $\overline{\text{RF}}$ signal is also sent to the PLL circuit where it is ORed with FSPS to control the $\overline{\text{G}}$ terminal. The reason for this is to keep the PLL in hold status when there is no RF signal, thereby preventing any possible

misoperation.
The microcomputer also checks $\overline{\text{FOCS LOCK}}$, $\overline{\text{FSLO}}$ and $\overline{\text{RF(SENS)}}$ periodically, and if the focus servo is effected by external vibration or shock during playback, pause, or search mode, the servo is stopped immediately.

The comparator reference voltage is about 2.1VDC.
And the RF rectifying voltage is

3.5V approx. during playback,
3.0V min. when scanning,
1.0V typ. when on the mirror portion,
and 0.8V typ. during stop mode.

4. PLL Circuit

This compact disc system employs a self-clocking system. The PLL circuit is locked by the clock component (4.3218MHz) of the edge information in the playback EFM signal, thereby obtaining a playback clock (PLCK). In this way, eight types of data P thru W are read, and this means that data can also be read even if SPDL is not completely locked. The information generated by playback clock and the information generated by the master clock are subjected to phase comparison, and spindle servo ø servo is applied to control the amount of jitter absorption RAM information. Although a narrow zone is preferred as far as the error rate is concerned, the intake time and consequently the search time are increased if the zone is too narrow. For this reason, the zone is widened as much as possible within the range where error rate does not deteriorate.

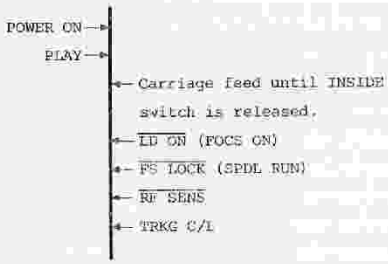
The next problem to be considered is how to cope with mislocking caused by lead-in and other fixed patterns. Mislocking prevents detection of the frame sync. If this happens, the spindle servo rotates so that the mislocked frequency becomes 4.3218MHz. In other words, if locked to spurious below 4.3218MHz, the actual rpm speed, or if locked to spurious higher than 4.3218MHz, the actual rpm speed will be slower than the correct rpm speed. And since this prevents data from being read, a means of restoring the system from these conditions must be considered.

With the singal (EFM I) activated by the leading edge of the playback clock (PLCK) obtained by dividing the VCO output by 4 serving as the output, the EFM signal (EFM2) converted to TTL level waveform signal by the ATC circuit is passed to the SYNC-SEPA & EFM SIG DEM IC Z1. The frequency error signal TMO (T MAX detect OUTput) is returned from Z1 to the PLL system.
The result of a NOR operation between $\overline{\text{RF}}$ and $\overline{\text{FSFS}}$ is applied to the input terminal $\overline{\text{G}}$ (held at LOW) used to keep the PLL in hold (open) status. When there is no RF or when in hunting status, the PLL is put into hold status to stabilize the PLL system when drop outs occur. (Up/down at HIGH impedance).

When in stand by mode, the externally applied control signal $\overline{\text{FSLOCK}}$ IN FOCUS ($\overline{\text{SP.RUN}}$ in the circuit) is at H level. Therefore, Z13 is ON, and EFM2 is LOW. The P/S pin of Z1 (pin 21) is switched to L (STOP), followed by the TMO pin (pin 48) being forced to switch to H. And since $\overline{\text{RF}}$ is H, the G pin of Z3 (pin 11) is switched to L. This results in the VCO oscillation frequency being set to the minimum frequency (about 13MHz).

When the PLAY button is pressed, the microcomputer shifts the carriage outwards until the INSIDE switch is released. As soon as the switch is released, the carriage stops, LD is switched on, and the "lens up" operation is commenced. The $\overline{\text{FS LOCK}}$ signal is supplied by SVCT Z3 once the focus has been locked. SPDL and PLL operations are started by this $\overline{\text{FS LOCK}}$.

The SPDL is accelerated in the forward direction by the play (H) signal for about 0.5 sec. The SPDL frequency servo is also started up by the play signal, and this, too, serves to accelerate the SPDL forward. When the SPDL commences to turn, the$\overline{\text{RF}}$ is detected, and $\overline{\text{RF}}$ detection results in the microcomputer switching TRKG to C/L.

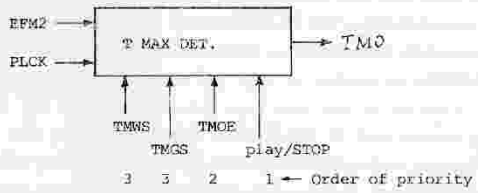


TMO description

The TMO is the result output of comparison between the EMP2 signal frequency information and the PLCK frequency. If the EFM2 signal obtained from the pick-up is lower than the playback clock, TMO is set to H to decrease the VCO. And if the EFM2 signal is higher than PLCK, TMO is set to L. When more or less equal, the three high impedance outputs are obtained. The TMO output conditions include the ① play/STOP (P/S), ② TMOE, and ③ TMGS and TMWS pins.

① P/S (play/STOP) play | STOP

Whenever stopping, TMO is always set to H and the VCO frequency is set to the lowest condition to enable easy loop entry.



② TMOE (T-MAX detect OUTPUT ENABLE)

The TMO output is switched to Hi-Z (high impedance) irrespective of the result of internal detection when an L input is applied to the TMOE pin. This circuit is connected to FSPS (which corresponds to GTOP in the P-D1) to prevent TMO output when in hunting status.

③ TMGS (T-MAX detect GATE SELECT)

To prevent output of TMO by mistake, the output is obtained only after high/low is detected a specific number of times in succession (seven when L and four when H). This pin is connected to the $\overline{SCAN}$ pin of the microcomputer, thereby giving added protection against the effects of misoperation

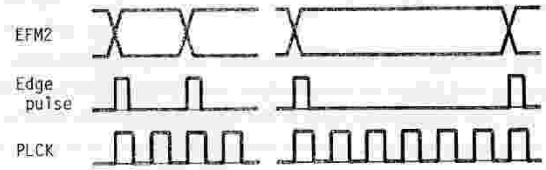
TMWS (T-MAX detection WINDOW SELECT)

When T-MAX is counted by PLCK:

		L	Hi-Z	H
TMWS	L	10PLCK	11PLCK	12PLCK
TMWS	H	10.5PLCK	11PLCK	11.5PLCK

This circuit is connected to $\overline{ATT}$, the zone being widened only when $\overline{ATT}$ is active. Normally, the zone is narrow. Consequently, 11±0.5 is used during playback, search, and pause mode, 11±1 being used only during output of the audio signal.

TMO generation involves the generation of input EFM2 leading edge pulses which are passed to a shift register where the edge intervals are counted by PLCK. The result when the maximum among 256 leading edge intervals is reached subsequently appears in the output. (588 / 2 = 294 > 256).



Although tracking becomes C/L (same as when OPEN), and the detected EFM2 signal is subject to wave forming in ATC before being applied to the PLL IC, rotation is still slow and the frame sync cannot be detected. FSPS also becomes H, Uo and Do are switched to Hi-Z, and TMO becomes H because of the slow rotation. In this condition, the SPDL servo operates so as to increase rpm speed after the internal sync (PLCK/58) iscompared with a reference for servo application purposes. Since TMO is H, PLCK moves in a decreasing direction, and is switched to Hi-Z when the difference from the EFM2 where the rpm

speed is increasing becomes zero.
If the frame sync is detected during this operation, FSPL becomes LOW, and the PLL IC commences PLL operations. If the spindle servo rpm speed is increased without detecting the frame sync, TMO becomes L, and PLCK is increased, resulting in the frequencies of EFM2 and PLCK becoming more or less equal. The frame sync is subsequently detected during this process. Where frame sync cannot be detected. the spindle servo applies f servo constantly to adjust PICK to 4.3218MHz. Consequently, servo is applied by TMO feedback to obtain a LIPLCK $\pm$ 0.5PLCK range, that is 4.3218MHz $\pm$ 196kHz, for the EFM. This can be thought of as much the same as the sync servo in the P-D1. And in reference to the PLL system, it can be considered similar to sweeping in the P-D1.

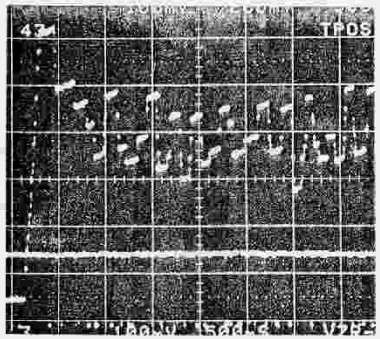
[Condition where frame sync pattern cannot be detected]
If this frame sync cannot be detected, the disc is rotated so as to adjust PLCK to the 4.3218MHz $\pm$ 200kHz range by the SPDL servo. This operation in effect makes EFM2 and PLCK approach each other, and when the difference is reduced to less than $\pm$51kHz, the freame sync can be detected.

[After frame sync pattern is detected]
When the frame sync pattern is detected, FSPS is switched to LOW (since RF is also naturally switched to LOW) and PLL operation is commenced.

The PLL consists of a phase comparator, a loop filter, and a VCO. Output of the result of phase comparisons is obtained from pin 7 (Up out) and pin 8 (Down out). The two output values from Up out (Uo) are Hi-Z and LOW level, and the two output levels from Down out (Do) are Hi-Z and HIGH lelel. In other words, when the PLCK phase is ahead of the EFM2 input phase, the Do pulse width is greater than the Uo pulse width, thereby resulting in the VCO phase being delayed. If on the other hand, the PLCK phase is delayed in respect to EFM2, the Uo pulse width is greater than the Do pulse width, resulting in the VCO phase being advanced. This operation is executed at each EFM2 edge.
The point of EFM2 change can be readily synchronized with the PLCK leading edge with the PLL in locked status by VR1 (PLL OFFSET) adjustment. (Variation exists in this voltage with different ICs and different sets, and has been found from experience to be about 2.7V for a Vcc of 5V).

Since EFM2 is a self-locking system, reading error is minimized when the EFM2 change point is synchronized with the PLCK leading edge. And VR1 is adjusted to cancel the offset due to differences between the Uo and Do output levels.
(Because of the high impedance at Uo and Do, note that the lock status can be released due to integration by capacitance when touched by probe etc. during normal status.)
The loop filter consists of R37,R38,R35,C16,R42, and C17 to ensure that the prescribed PLL characteristics are attained. When Uo is L, an inverse phase input is applied to pin 2 of Z3, resulting in pin 4 becoming H and the VCO oscillation frequency being increased. And if Do becomes H, pin 4 becomes L and the VCO oscillation frequency is decreased.
The VCO is a clamp type oscillator where oscillating frequency is altered by capacitance changes in the D3 variable capacitor. The VL1 variable coil is adjusted to obtain a frequency of $4.3218 \times 10^6 \times 4 = 17.2$MHz when the voltage on pin 1 of Z6 is about 5V. When the PLL is locked, the oscillation level at the emitter of Q7 is about 0.5Vp-p (typ.).

[Release from mis-lock condition]
The EFM signal becomes a fixed pattern at unrecorded sections such as at lead-in, lead-out, and between tunes, and a strong frequency spectrum is generated in the vicinity of clock frequencies in addition to clock components. In this case, the frame sync pattern cannot be detected. This fact is utilized in the P-D1 to release mis-locked conditions by forced sweeping with GTOP at H.
When a mis-locked condition occurs in the P-D70, the FSPS (Which corresponds to the P-D1 GTOP) is switched to H, resulting in the PLL being held and the mis-locked condition cancelled by SPDL "disturbance".

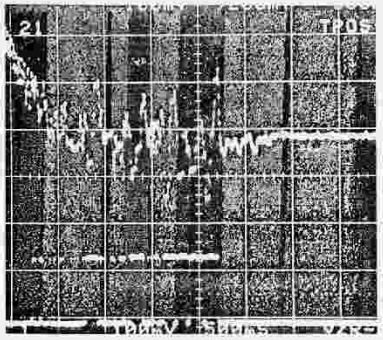


Power on → Playback

$\overline{G}$ is forced to L, FSLO is fixed to L by control, and PLL sweep and FSPS status is checked by TMD.

Top: PLL 1V/div
Bottom: FSPS 2V/div
H: 500ms/div

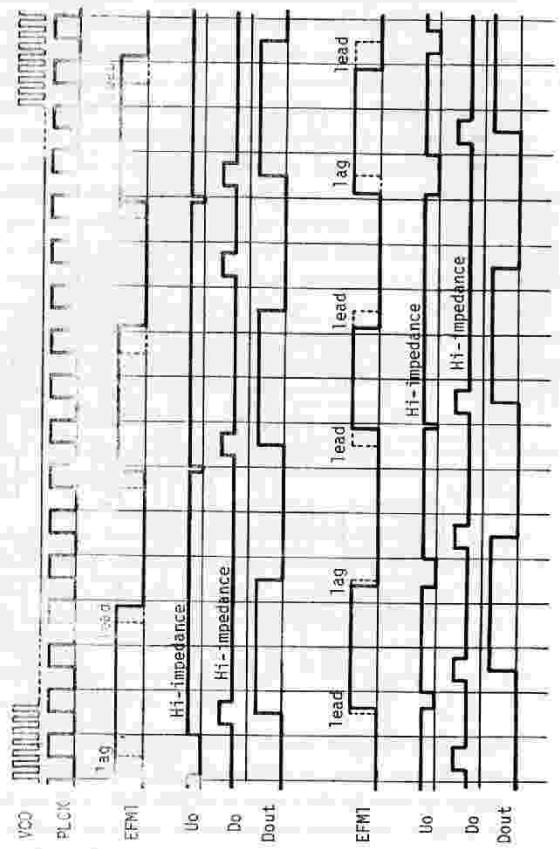
Typical sweep time : 30ms approx.



Power on → Playback
Normal circuit
Top: PLL 1V/div
Bottom: FSPS 2V/div
H: 500ms/div

SPDL is accelerated and when the 13 MHz vicinity is reached, the sync lock pattern is detected (FSPS:L), data is read, and a multi-jump search is made. The TOC is read and number 1 search/play is executed.

TD6315P TIMING CHART



5. SYNC-SEPA & EFM Signal Demodulation

The major features of Z1 (TC9178F) are listed below.

a. Frame sync pattern detection, protection, and insertion

b. EFM demodulation

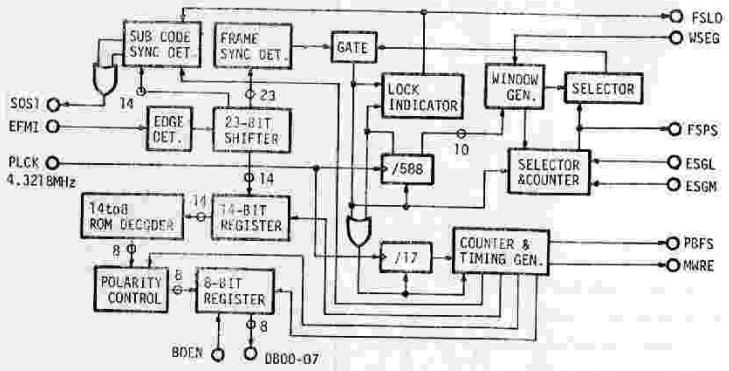
c. Sub-code demodulation

d. CLV control signal generation (AFCO, APCO)

e. PLL control signal generation (TMO)

(This device handles all the functions of the CX-7933 and half the functions of the CX-7934 used in P-D1).

a. Frame sync detection



Reading of the EFMI signal is executed by the PLCK trailing edge in this IC, but since the EFMI signal is data reproduced from disc, any change in data in the vicinity of the PLCK trailing edge due to drop out or similar occurrence may result in incorrect reading of the data. Therefore, the phase of the PLL output is adjusted so that the PLCK leading edge comes at the center of the position where EFMI changes can occur. So after latching the EFMI data at the PLCK leading edge, the data is read at the PLCK trailing edge.

The EFMI signal read in this way is first converted into an NRZ signal with changed data points as 1 and other points as 0, and is then passed to a 23-bit shift register where a resultant parallel output is passed to the frame sync detector.

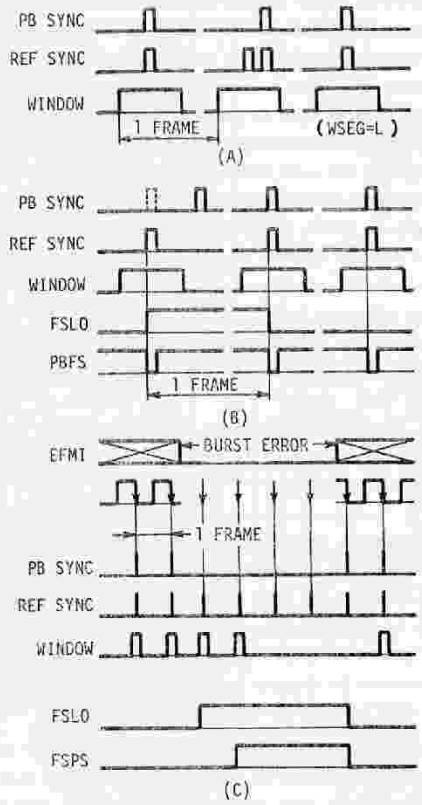
After the detected frame sync is applied to the gate with a fixed detector window, it is compared constantly with an internal counter sync which divides PLCK by 588. When the frame sync is within the detector window but there is clock displacement (bit slip) between EFMI and PLCK, the counter sync is preset forcibly to the frame sync to prevent continuation of the misaligned status. The counter sync is thus generated at the same timing from the next frame sync (see Fig. (A) below). The width of the detector window can be altered by the voltage applied to pin 42 (WSEG, H: ±7 PLCK, L: ±3PLCK).

Although the counter sync is always generated once at the 588th PLCK count, the sync pattern may not always be detected due to drop out etc, and the frame sync may fail to be generated. If this happens, the FSLO pin (pin 55) is switched to H only during that frame. The counter sync output is subsequently obtain without any special operation being executed (see Fig. (B)).

If, however, there is a very large displacement from the expected position, and the frame sync is generated outside the detector window, that sync is disregarded.

If the frame sync is displaced from the detector window for X frames, pin 51 FSPS is set to I and the internal counter sync is preset at the timing of the next frame sync (see Fig. (C)). Presetting of this counter sync is executed irrespective of the detector window position (the window generator output selector being switched by FSPS).

These X frames can be changed to any number from 2 thru 12 by input of ESGL and ESGM to pins 45 and 46.



The mechanism used to protect these frame syncs is switched to single frame feed and other modes. Single frame feed is strengthened against bit slip and drop out by a detector window width of ±7 bits and a frame protection interval of 12 frames. And during search operations where the target address is approached while reading addresses, the detector window width is narrowed to ±3 bits and the frame protection interval is reduced to 2 frames to avoid locking incorrect syncs due to drop out, and to enable rapid release from incorrect sync lock status if such a sync is locked.

Once the frame sync can be detected, the frame frequency (7.35kHz) PBFS signal and the MWRE signal which counts 17 PLCKs and divides the frame into symbol units are obtained as outputs after synchronizing with the internal counter sync.

b. EFM demodulation

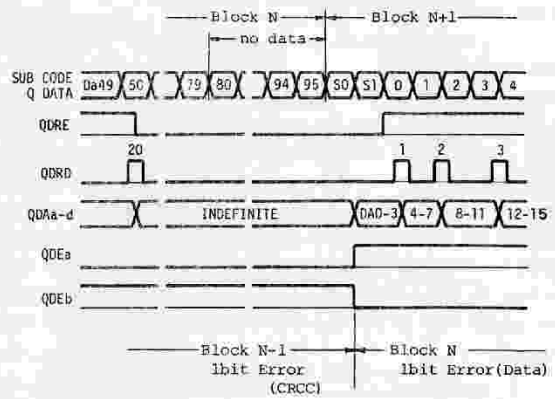
Although a separate output from the 23-bit shift register is passed to a 14-bit register, data is latched one symbol at a time at MWRE timing. This latched data undergoes a 14 -- 8 conversion in the internal ROM, thereby demodulationg the data one symbol at a time to the same original 8-bit data as before EFM modulation. Each symbol apart from the control data is passed to an 8-bit register connected the data bus in preparation for RAM writing. The register output (data bus) is three-state, the output being placed on the bus when the enable signal BOEN is 0. In other cases, the output is at high impedance.

c. Sub-code demodulation

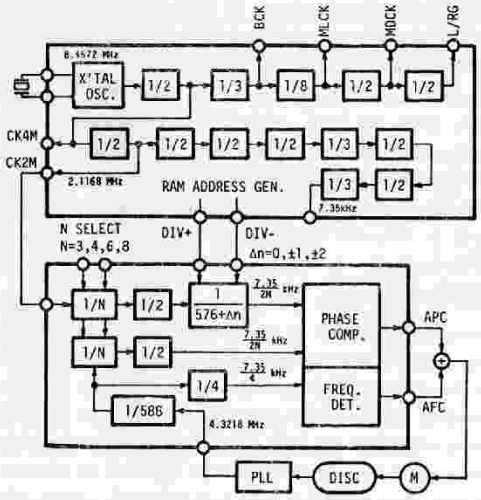
Although the control data forms one block every 98 frames, the sub-coding syncs S0 and S1 which denote the partition between blocks indicate specific patterns which are detected by a sub-code sync detector. Even if that signal can only detect S0 or S1 the sub-code Q output is synchronized by the S1 timing if FSLO is at L.

Data transfer with the microcomputer is executed in six signal lines QDAa thru QDAd, QDAS, and QDRD. When the microcomputer is at the timing for data reading, QDAS is changed to L and QDAa is read. An H level indicates that new data has been set. An H level in QDAc as a result of a CRC check thus indicates that there are no errors in the data, and with QDAS at H, a 20-pulse input is applied to QDAD to enable 4x20 = 80 bits of data to be read. In this way, the number of tracks, index number, MIN SEC, etc is read.

Subcode Q Data Read Timing Chart



d. CLV control signal generation



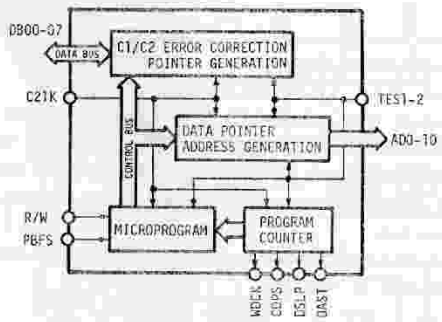
One of the features of the CD player is the absence of wow and flutter in the reproduced sound. This is achieved by regular D/A operations based on a stable crystal oscillator master clock. In other words, playback data obtained from the rotationg disc where wow and flutter is generated is written in a RAM based on the playback frame frequency, and then read out again at timing obtained by dividing the master clock, thereby eliminationg the wow and flutter components.
This necessitates the application of a phase servo to match the phases of the playback and master clocks to avoid excesses and deficiencies in the RAM information. Therefore, phase servo is applied by dividing the master clock by the playback sync (PBFS) (using a division factor N of 12 where 7.35kHz/12 = 612.5Hz). RAM status is monitored by the DIV+ and DIV- pins of Z2 (TC9179F), feedback being applied if the jitter absorption memory occupies ±3 frames out of ±4 frames, the phase servo being applied so as to absorb the jitter. The control signal involved in this operation is APCO. Since suitable dumping characteristics cannot be obtained by phase servo alone, the spindle motor is driven after mixing with a frequency error signal (AFCO). Since both the AFCO and APCO outputs are pulse width modulated, the mixing follows rectification by fc = 340Hz secondary Butterworth A.P.F.

6. Error Correction and Jitter Absorption

The main functions of Z2 (TC9179F) include jitter absorption from the 32 symbols of data received from TC7178F, generation of address signals for the RAM where de-interleaving is executed, C1 and C2 error detection and correction, and average value compensated data output control of data which cannot be corrected.
(This device handles half the functions of the CX-7934 and all the functions of the CX-7935 used in P-D1).

Data is received via the data bus shown in the accompanying diagram, the read/write control at that time being controlled by the R/W signal. The data address resets the program counter at the trailing edge of PBFS, and sets the microprogram to the start address, the addresses Ad0 to Ad10 being passed to the RAM address. At the same time, error detection and correction calculations are executed by C1 and C2 CIRC codes. If corrections

are to be made after completing calculations, the relevant data and addresses are passed to the RAM where the RAM data is rewritten. The error status at that time is written at a pointer corresponding to the RAM data, resulting in the error data and addresses also being passed to the RAM where they are rewritten. And the monitor output which checks whether corrections are executed or not appears at DAST.
The C1 error correcting decoder can correct errors in up to two symbols out of the 32 symbols of data per frame. The correction is made in symbol units of eight bits of data. Since one frame of interleaving is applied per symbol as the recording signal, five symbols of error data will exist in one frame on the disc, and error correction by the C1 decoder is no longer possible. In other words, if there are more than 56 channel bits (approx. 13μs, or approx. 16μm at 1.25m/s linear speed) of drop out, correcting by the C1 decoder is not possible.
Where there are two incorrect symbols in one frame, error pointers are placed in all 28 symbols apart from the frame P parity since incorrect correcting is also possible at the same time that errors are corrected. Although correction is not executed if there are errors in more than two symbols, error pointers are placed in all 28 symbols. The error logic table for errors detected by the C1 decoder is given in the following diagram.



No. of error symbol	C1 data correct.	No. of C1 pointer
0	none	all 0
1	1symbol correct.	all 0
2	2symbol correct.	all 1
more than 2	none	all 1

The C2 error correction decoder is capable of correcting errors in up to three symbols in a single correction block (28 symbols) excluding the C1 correction P parity. The correction operation is executed in the same way as in the C1 decoder, and use of C1 error pointers detected by the C1 decoder enables more accurate corrections to be made. In C2 correction, 28 symbols of data per frame is subject to four frames of de-interleaving between each symbol.
Therefore, one symbol of error per frame can be corrected by the C2 error correction decoder even for drop outs of up to 12 frames in length (approximately 2.04mm at a linear speed of 1.25m/s) in the recorded signal on disc.

An external crystal resonator and capacitor are added to the master clock generator, resulting in the generation of an 8.4672MHz master clock signal (CK4M). This clock signal serves as the basic clock for RAM control, C1 error correction, C2 error correction, interpolation, and other functions.
All data is written to and read from the RAM via the common data bus. The RAM is accessed by a data write request.
RAM accessing for writing and reading for CIRC correction code decoding (C1 and C2), RAM accessing for reading data while de-interleaving, and RAM accessing involving priority control and actual RAM addressing for these RAM access request is executed. The request to write data into the RAM from TC9178 is executed by MWRE. When MWRE is passed from TC9178 to TC9179, BOEN is returned in response to enable output of TC9178 data, and R/W CE1 is passed to the RAM to put the RAM into data write status.

Although RAM data writing is executed in symbol units, data for C1 and C2 corrections is read from RAM to TC9179 following RAM data writing during a single write cycle. Reading of data for this purpose is achived by sending R/W from TC7179 to the RAM. The RAM addressing on this occasion involves sending the address specified by the RAM address generator in this IC to the RAM. When error data is corrected, the correct data is rewritten at the address where the error data is stored, and the error pointers indicating the results of the correction are written. The data and error pointers where C1/C2 correction has been executed are read from the RAM into the TC9179 interpolation circuit via the data bus.

Errors which cannot be corrected by the C2 correction section are passed onto the interpolation or previous value hold sections. Data which still cannot be corrected is subsequently subjected to a combination of direct averaging and previous value hold as indicated in the following table, depending on the status of the data.

Ln+1			Ln			Output Data	
MSB -30dB	MSB C2Ep	LSB C2Ep	MSB -30dB	MSB C2Ep	LSB C2Ep	Process	Contents
X	0	0	X	0	0	Ln	Direct
X	X	X	0	0	1	Ln(MSB-80)	Direct
X	0	0	X	1	X	(Ln-1/2)+(Ln+1/2)	Average
0	0	1	X	1	X	(Ln-1/2)+(Ln+1(MSB-80)/2)	Average
1	0	1	X	1	X	Ln-1	Pre-value
X	1	X	X	1	X	Ln-1	Pre-value
X	0	0	1	0	1	(Ln-1/2)+(Ln+1/2)	Average
0	0	1	1	0	1	(Ln-1/2)+(Ln+1(MSB-80)/2)	Average
1	0	1	1	0	1	Ln-1	Pre-value
X	1	X	1	0	1	Ln-1	Pre-value

∇ MSB -30dB ----- Flag indicating that MSB 8-bit data is greater than -30dB from the maximum level or not "1" indicates that it is greater.
∇ MSB C2Ep ----- C2 Error Pointer from MSB side "1" ; error
∇ LSB C2Ep ----- C2 Error Pointer from LSB side "1" ; error
∇ MSB-80 ----- LSB side data is "1000 0000" ; Central value of 8-bit code

Although this LSI is capable of both parallel and serial output of D/A coverter data, since the P-D70 employs a serial-in D/A converter, the P/S SE pin is set to H level for 16-bit serial output.

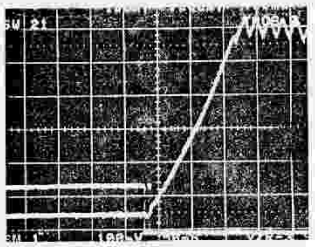
When a 64-frame burst error and jitter absorption memory "buffer over" status are detected by the mute signal detector circuit, -14.5dB attenuation is applied to the output ($\overline{AT-3}$)/($\overline{MUT-01}$). And 12dB attenuation is also applied digitally during audio output FF and FR modes. ($\overline{AT-0-2}$) In this case, data compensation is switched to partial compensation (ALGC pin) to minimize deterioration in the quality of sound.

In addition, the microcomputer monitors FSLO, and if it remains at H for 16 consecutive frames during playback, $\overline{MUT-1}$ is set to L and ∞dB of digital muting is applied. And if it remains at L for 16 consecutive frames, muting is cancelled. Muting is applied momentarily during search, pause, and stop modes.

7. Disc Drive

C40 is charged up by the $\overline{IN\ FOCUS}$ signal during stand by as indicated in the diagram. When $\overline{IN\ FOCUS}$ is executed, the voltage on pin 3 of Z8 is dropped to -3V by C40 discharge, and the spindle motor is accelerated for about 0.5sec (Which corresponds to the time constant). The Z1 frequency servo operation is started by the $\overline{IN\ FOCUS}$ signal (but the phase servo APCO still remains inactive and the pattern is fixed at duty 50% at this time). The EFM2 frequency applied to Z1 is still low at this stage, and the sync pattern cannot be extracted. Consequently, the output PBFS (pre-bank frame sync) is obtained by dividing PLCK by 588, and since the PLCK is fixed at the minimum frequency by TMO at this stage, the frequency is 13MHz ÷ 4 ÷ 588 ≒ 5.5kHz < 7.35kHz. Consequently, the frequency error AFCO operates so as to increase the rpm speed, that is, to shift duty towards H.

As the spindle is accelerated, the EFM2 frequency is increased. And when the EFM2 clock frequency is increased passed the frequency fixed by TMO, the TMO commences operation. The frame sync pattern is subsequently detected, FSPS is switched to L, and PLL operation is started.
Although the frame sync pattern and the playback PBFS are detected, the PBFS frequency is also lower than 7.35kHz, and together with the accelerator circuit, the SPDL is rotated in the accelerating direction.
When the playback PBFS reaches 7.35kHz ± 5%, DMLD (disc motor lock detect output) is set to H and the phase servo commences to operate.



Power on Playback

Top: PLL 1V/div

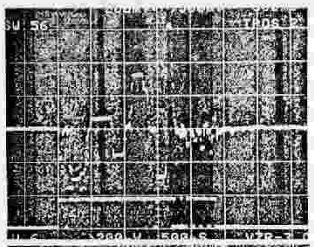
Bottom: FSPS 2V/div

H: 50ms/div

FSLD pratically the same.

The phase servo is switched on within $\pm$ 5% and is reset within $\pm$ 10%. Therefore, when the VCO control voltage is considered, $7.35 \times 10^3 \times 4 \times 588 \times 1.1 = 19 \times 10^6$ Hz, approx. 5 $\pm$ 2.4V ; lock-out, $7.35 \times 10^3 \times 4 \times 588 \times 0.9 = 15.6 \times 10^6$ Hz, approx. 5 $\pm$ 1.2V ; lock-in can be considered.

When PBFS is detected and acceleration is increased, PBFS exceeds 7.35kHz, resulting in a change to deceleration. As was mentioned earlier, since reading is possible as long as Q DATA locks PLCK and EFM2, data is read and TOC search mode is activated by this process.

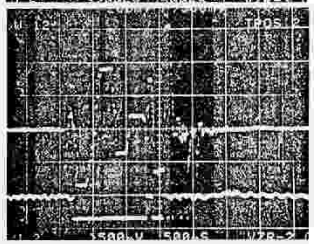


Top: PLL 2V/div

Bottom: FSPS 5V/div

H: 500ms/div

Inside to outside search



Top: PLL 2V/div

Bottom: CARG DRIVE

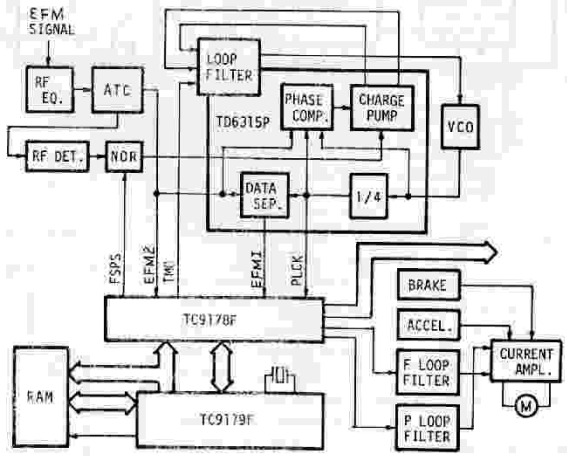
H: 500ms/div

Inside to outside search

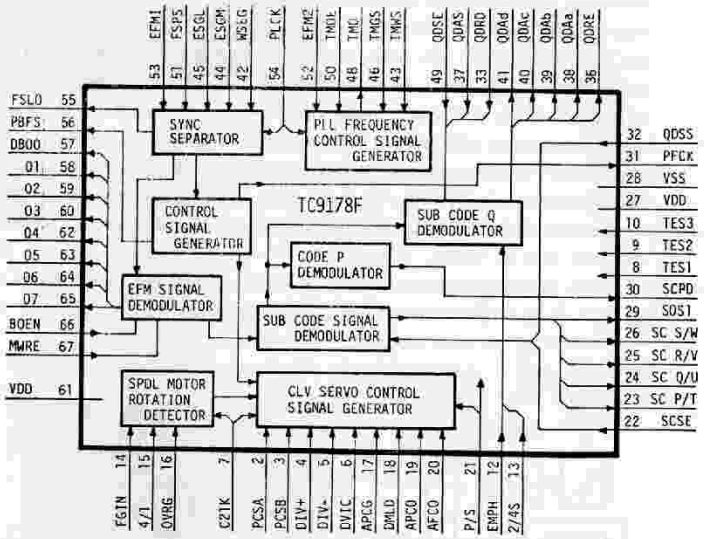
During search sequences, the carriage is moved to the target address by track counting. TRKG is O/L at this time, and carriage movement is fast. PLL operation, therefore, is controlled by TMO. In this status, SPDL rpm speed can be changed, if somewhat roughly. If the carriage stops, the frame sync pattern is detected, DATA is read, and the next search is started involving multi-jump and playback.

When in stop mode, the IN FOCUS signal is set to H. As a result, AFCO is set to L and APCO to 50% duty. Although the P-D1 was equipped with a short brake for stopping and a mechanical brake for eject purposes, the P-D70 is equipped with an electrical brake (and has no mechanical brake). When IN FOCUS is at H, D12 is cut off, and Q11 is turned on while C41 is being charged up (time constant of (R70+VR3)//(R71)). Since AFCO is low at this time, a counteracting brake is applied to the SPDL at this time. VR3 is used to equalize the stopping time at the inside and outside tracks when the SPDL load is light.

If focus is lost due to shock being applied to the set, the SPDL is started by a start-up sequence to ensure proper operation.



DCDR BLOCK DIAGRAM



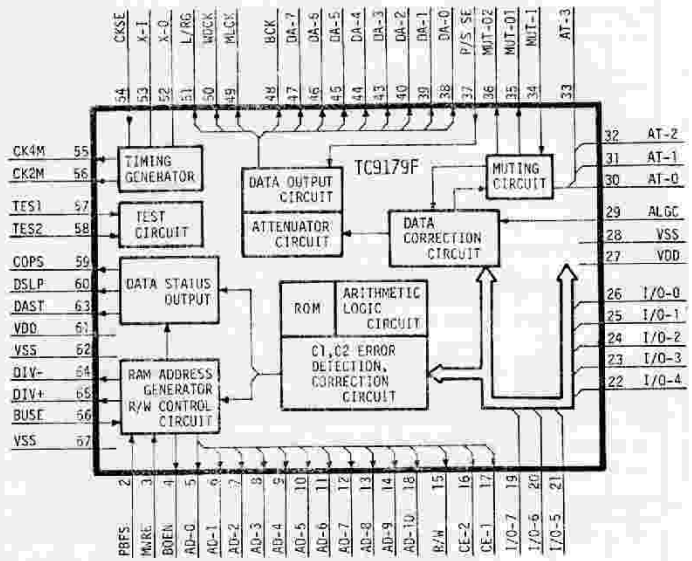
TC9178F Pin Functions

Pin No.	Pin Name	I/O	Function
2	PCSA	I	Phase comparate selector inputs.
3	PCSB	I	Pins for selecting the phase comparison frequency for the APC signal generator circuit used in CLV servo control. Since PCSA is "L" and PCSB is "H" in P-D70, the selected frequency is 612.5Hz.
4	DIV+	I	Control input signal for increasing the phase comparison reference frequency in the CLV servo control APC generator. Connected to TC9179F DIV+(65p).
5	DIV-	I	Control input signal for decreasing the phase comparison reference frequency in the CLV servo control APC generator. Connected to TC9179F DIV-(64p).
6	DIVC	I	Divider Control Input. Selection of the variable quantity which controls the above frequencies. Connected to GND in P-D70. 1/288 ± 0.5 if pin is "L" and 1/288 ± 1 if "H".
7	C21K	I	2.1168MHz clock input. Connected to TC9179F CK2M(56p).
8	TES1	I	Test input pin. Normal operation when pin is at "H" level or when open.
	" 2	I	
10	" 3	I	
12	EMPH	O	Emphasis status decision output. De-emphasis is ON when pin is at "H" level.
13	2/4S	O	2/4 audio channels switching decision output. 2 channels when at "L" level, 4 channels when at "H" level.
14	FGIN	I	Spindle motor FG pulse input pin. Connected to GND in P-D70.
15	4/1	I	Selection of 1 or 4 FG pulses per revolution. Connected to GND in P-D70.
16	OVRG	I	Selection of whether FG is to be used or not. Not used when pin is at "L" level. Connected to GND in P-D70.
17	APCG		APC Control Gate Input. Input pin for switching CLV servo control APC generator ON and OFF. When at "L" level, generator is switched off, and the APC output is fixed to zero phase difference (50% duty).
18	DMLD		Spindle motor lock detector output. Pin is switced to "H" level when set by the FF output which is set when the frame sync signal frequency is found to be within ± 5% (or reset if the frequency is found to be greater than ± 10%). By being connected to APCG, the output is used in APC block control.

TC9178F Pin Functions

Pin No.	Pin Name	I/O	Function
19	APCO	O	APC signal output pin. Output signal is obtained as PWM (Pulse Width Modulation) signal.
20	AFCO	O	AFC signal output pin. Output signal is obtained as PWM (Pulse Width Modulation) signal.
21	P/S	I	Play/Stop select input. Pin for switching the CLV servo control signal on and off. Pin is set to "H" level during playback, and to "L" level during stop mode, resulting in the AFC output being fixed to "L" level and APC output to 50% duty.
22	SCSE	I	Sub-code signal data switching input. "L" level for output of P, Q, R, and S 4-bit data, and "H" level for output of T, U, V, and W 4-bit data.
23 24 25 26	SCPT SCQU SCRV SCSW	O	Output pins for output of the eight bits of sub-code signal data P, Q, R, S, T, U, V, and W. Output of the four bits of data in this signal is obtained one bit at a time by the SCSE signal data in each frame. Data switching in each frame is synchronized with the trailing edge of the PFCK signal.
29	SoSl	O	Sub-code Sync detection output when the sub-code sync pattern S0 or S1 is detected, the pin is switched to "H" level during that frame interval.
30	SCPD	O	Output indicating the data contents of sub-code signal P. This output is the result of checking the data in each frame at every five frames by the detector section.
31	PFCK	O	50% duty (approx) signal output for each frame. Sub-code data is switched after synchronizing with the trailing edge of the output.
32	QDSS	I	Selection of sub-code sync pattern detector mode for sub-code signal Q demodulation. Connected to GND in P-D70.
33	QDRD	I	Q-data read signal input. Pin used in reading sub-code signal Q data in 4-bit units from the QDAa thru QDAd outputs. When this pin is changed back to "H" level, the next four bits of output data are set in QDAa thru QDAd after a fixed period of time from that "H" level edge.

Pin No.	Pin Name	I/O	Function
36	QDRE	O	Sub-code signal Q read enable signal output. Upon completion of error judgement on the input sub-code signal Q, the four bits of data at the MSB end are set in QDAa thru QDAd, and the output is switched to "H" level to enable read out. Not used in P-D70.
37	QDAS	I	QDAa thru QDAd output data switching input. Output of the Q signal block error judgement results (QDEa and QDEbsignals) and the QDRE signal when at "L" level, and output of Q data in four bit units when at "H" level.
38 " " 41	QDAa b c d	O	Three-state Q data and block error judgement result outputs.
42	WSEG	I	Window Select Gate Input. Gate signal window selector pin for determining whether the frame sync pattern is to be applied as the internal system sync signal or not when that pattern is detected. ± 3 when at "L" level (PLCK clock count), and ± 7 when at "H" level.
43	TMWS	I	T-max detection window select input. Input which selects N in Tmax = N (PLCK) upon detection of the input EFM Tmax from EFM2. 11 ± 1 when at "L" level, and 11 ± 0.5 when at "H" level.
44	ESGM	I	Error frame sync Select Gate L and M
45	ESGL	I	When the frame sync pattern is not detected after N consecutive frames within the frame sync protector gate signal window, each system is synchronized by the frame sync pattern out side the next input window. This N is selected by these two input pins. 12 when at "L" level, 2 when at "H" level.
46	TMGS	I	Tmax detector gate select input. To prevent misdetection of fmax, the data is used when N times of consecutive Tmax are detected. N = 7 when at "L" level, and 4 when at "H" level.
48	TMO	O	Tmax detector output.(three state) This output is used to control PLL circuit. When at "L" level, f f When at "H" level, f f When at "high-impedance-state", f = f
49	QDSE	I	When at "L" level, QDAa thru QDAd outputs are in the high-impedance-state.
50	TMOE	I	When at "L" level, TMO output is in the high-impedance state.



Pin No.	Pin Name	I/O	Function
50	TMOE	I	When at "L" level, TMO output is in the high-impedance state.
51	FSPS	O	Frame sync pattern synchronizing output. When the frame sync pattern is not detected after 8 consecutive frames, this output turns to "H" level.
52	EMF2	I	EFM signal input from ATC comparator.
53	EFMI	I	EFM signal input from PLL circuit.
54	PLCK	I	PLCK input from PLL circuit.
55	FSLO	O	Frame sync lock detector out. When the frame sync pattern is detected this output turns to "L" level.
56	PBFS	O	Play-back frame sync output. When at "H" level, demodulated data are transferred to TC9179F.
57 58 59 60	DB07 " 6 " 5 " 4	O O O O	Three-state data output pins.
62 63 64 65	DB03 " 2 " 1 " 0	O O O O	
66	BGEN	I	Bus out enable input. When at "L" level data bus is enabled.
67	MWRE	O	Memory write request output. Indicate the status if data bus is ready to write in RAM or not. turns to "L" by the set timing of Data-transfer-register of data bus and this turns to "H" when BOEN signal turns to "L". After PBFS signal turns to "H", data appears 32 times in every 17-clock of PLCK

Pin No.	Pin name	I/O	Function
2	PDFS	I	Frame synchronization input pin. Input of frame symbol interval signals from TC9178F. Connected to TC9178F EFFS (pin 56)
3	MWRE	I	Memory write request input. Input of MWRE signal from TC9173F. Connected to TC9178F MWRE (pin 67)
4	BOEN	O	Bus output enable output. Output of control signal which switches the symbol data output pins (DB0 and 0, thru 7) on when reception of the MWRE signal from TC9173F has been enabled. Connected to TC9178F BOEN (pin 66)
5 – 14	AD-0 – AD-9	O	RAM address outputs connected to external RAM (8 bits + OK) address pins.
15	R/W	O	Read/write signal output connected to RAM R/W pins. "H" = WRITE, "L" = READ
16	CE2	O	Chip enable signal output which appears when correction data is written in external RAM during C2 correction.
17	CE1	O	Chip enable signal output which appears during external RAM read/write. This output is connected to RAM CE1.
19 – 26	I/O-7 – I/O-0	I/O	Input/output pins for data transfer with RAM and TC9178F. Connected to RAM I/O-0 thru I/O-7 and TC9178F DB00 thru DB07.
29	ALCC	I	C2 correction process selector pin. This pin selects the processing algorithm for frames where error symbol detection is not possible in the C2 correction section. Pin is switched to "L" during playback mode. When at "H" level, the error indicator signal detected at the C1 correction section is passed to

Pin No.	Pin name	I/O	Function
			the compensation processing section as the C2 section indicator signal.
30 – 33	$\overline{AT-0}$ – $\overline{AT-3}$	I/O	Digital attenuator input/output pins. Internal digital ATT level monitor and external control pin. These pins become output pins (monitors) when WDCK = "L", and input pins (external control) when WDCK = "H".
34	$\overline{MUT-I}$	I	Muting control pin. Internal digital ATT automatic control section control pin. ATT level increased when pin is "L" (finally becoming digital "0"), and decreased when pin is "H" (shift towards 0dB side).
35	$\overline{MUT-O1}$	O	Muting 1 output pin. Pin is switched to "L" if burst error of more than 64 frames, or if "buffer over" in the jitter absorption memory (RAM).
36	$\overline{MUT-O2}$	O	Muting 2 output pin. "L" level output if three consecutive frames of de-interleaving error is detected.
37	$\overline{P/S\ SE}$	I	Output data parallel/serial selector pin. Serial output operation when pin is at "H" level. Set to "H" level in P-D70.
38 – 46	DA-0 – DA-6	O	Not used in P-D70
47	DA-7	O	Serial data output from MSB end
48	BCK	O	Bit clock output for output of serial data to Serial data output is synchronized with the trailing edge of this signal. (1.411MHz)
49	MLCK	O	MSB/LSB clock output. This clock output which divides SCK by 8 is used as the setting clock during output of 8-bit parallel data.

TC9179F PIN FUNCTIONS DATE

Pin No.	Pin name	I/O	Function
50	$\overline{WDCK}$	O	Word clock output. This clock output which divides BCK by 16 indicates the single word output interval
51	L/RG	O	Sampling frequency output. This clock output which divides WDCK by two indicates L/R channel of the data output. "L" = L channel, "H" = R channel.
52	X-O	O	Crystal oscillator connector pin. 8.4672MHz.
53	X-I	I	
54	CKSE	I	Clock select pin. 8.4672MHz when at "H" or open, 4.2336MHz when at "L".
55	CK4M	O	4M clock output
56	CK2M	O	2M clock output. The TC9178F clock is obtained from the 2.1162MHz output pin. Connected to TC9178F C21k (pin 7)
57	TES1	I	Test pins which are normally at "H" or are open.
58	TES2	I	
59	COFS	O	Frame sync output pin.
60	DSLP	O	Data status latch signal output.
63	DAST	O	Data status output. Bit-serial output of the jitter absorption memory buffer contents and the C1 and C2 detection results. Monitor enabled when connected to external latch circuit.
64	DIV-	O	Buffer-up output. "H" output when in the +2 or +3 frame area of the jitter absorption memory buffer capacitance ±4 frames. This output is connected to DIV- of TC9178F to lower the spindle motor rpm speed. Connected to TC9178F DIV- (pin 5)
65	DIV+	O	Buffer ~~counter~~ down output. Motor rpms in this case are increased. Connected to TC9178F DIV+ (pin 4)
66	BUSE	I	Buffer select input which selects DIV-/DIV+ output conditions. ±2 frame area when "H", and in ±3 when "L".

Outline of Optical System

1. Optical Path and Optical Components

Fig.1 is an outline of the optical path through the optical components in the pick-up mechanism. This path is described in detail below.

At 780nm, the beam of light emitted from the laser diode lies just within the visible range. The beam of light from the very small light source forms a conical shape with an elliptical cross-section. In order to provide beams for tracking error detection, the light is passed through a grating where it is split into three separate beams - 0 order and ±1 order. Although most of the light energy is kept within these three beams, there is a small amount of light lost due to higher order diffraction. The beams are then passed through a half-prism where half the quantity of light is lost before being directed towards a collimator where the beams are made parallel. The diameter of the light beam at this stage is sufficiently large to cover movement of the object lens. The light converged into a very small spot by the object lens is subsequently reflected/diffracted at the disc surface and is passed back through the object lens where the light again forms parallel beams. This

beam is passed back through the collimator where the beam is converged, and is then passed through the half-prism. Half of this light is then passed through the grating to reach the laser diode. The other half of the light reflected at the half-prism is passed through a concave lens and a cylindrical lens used for focus signal detection purposes to reach a photo diode array where changes in the intensity of light are converted into electric signals.

Comparisons with the laser disc optical system reveal a number of different characteristics. These characteristics are described below in further detail.

The first characteristic is the linearity of the forward path as shown in the diagram. This minimizes the tolerance and enables optical system adjustments to be reduced to a minimum. This has been made possible by reduction in the size of the object lens after perfecting a dual-axis actuator for the parallel drive system, and further miniaturization of the optical components without sacrificing performance.

The second characteristic is the half-prism. The forward and return paths in previous systems were separated by using a 1/4 wavelength plate in combination with a polarizing beam splitter (prism). Despite the loss of a

considerable quantity of light, there are three good reasons for using the half-prism. (1) The laser diode output power is some three to five times greater than He-Ne tubes. (2) Unlike He-Ne tubes, noise generated in laser diodes is kept at a low level up to a certain point of return of the light beam. (3) The differences between the DAD and laser disc specifications. In both cases, the disc is made of a resin material, and warping of the discs results in polarization of the light. The restrictions placed on this polarization are less stringent for DAD, and there is little point of using a highly accurate 1/4 waveform plate if there is considerable variation between different discs in the first place. When a half-prism is used, there is no deterioration in the performance of the optical system due to polarization, no matter what kind of disc is loaded.

The third characteristic is the ability to read signals under the same optimum conditions by the parallel drive unit without any change in the performance of the object lens. As can be seen in Fig.2, the light from the laser diode is collimated into perfectly parallel beams by the collimator lens. The parallel drive unit ensures that the object lens remains perfectly perpendicular to the optical axis while making lateral or perpendicular movements. The

object lens shows no change in performance at all as a result of these servo mechanisms as long as the lens remains within the range of the light beams.
The fourth characteristic is the use of the concave lens which prevents any reduction in the focal depth on the photo diode as a result of the compact design of the optical system. This lens also contributes to the optical system stability by requiring less precision in the position of the photo diode.

2. EFM Signal and Servo Signals

The role played by the focussing and tracking servo signals in the optical path is of great importance. The detection of the focussing servo signal is achieved by a focus servo signal detector system based on the use of a superb cylindrical lens developed through Pioneer's many years of experience in laser disc player manufacturing. And the tracking servo signal detection system involves splitting the light into three separate beams by a grating to absorb variations between different discs in the most effective way conceivable. One of the basic items considered when designing the optical system was how to cope with disc variations. With a wide range of disc manufacturers, careful consideration was given not only to

variations within the same disc brand, but variations between different manufacturers. This is why an object lens N.A. of only 0.45 has been selected even though a laser diode of only 780nm (which is the shortest wavelength possible in currently mass-producible devices) has been adopted. And although the reduction in the EFM signal level is practically proportional to the N.A. even under the worst possible conditions, it still lies within the range where adequate compensation by the E system equalizer is possible. On the other hand, aberration due to disc variations which can lead to deterioration in the optical system performance, is generated in proportion to $1/NA^2$, $1/NA^3$, $1/NA^4$, etc. The NA = 0.45 specification was finally decided after conducting various simulation calculations and experiments.

The beam of light which forms a very small spot after passing through the object lens is directed into pits formed in the signal plane (disc surface). The light which is then reflected/diffracted at the signal plane is passed back through the object lens to a photo diode where the information contained in the signal plane pits is converted into electric signals. The operation is described in further detail below.

A look at Fig.3 shows the converged spot directed onto the pit in 3(A), and between adjacent pits in 3(B). When the spot is on a pit as in 3(A), the light is diffracted (although the diagram only shows typical diffraction directions, there is high order diffraction of light to both left and right, and forward and backward), and the light in the shaded area is not returned to the object lens. Only the central portion is passed back through the object lens to the photo diode. The returned light, therefore, is "weaker" and corresponds to "dark" information. When the converged spot is directed onto the flat area between pits as in 3(B), on the other hand, there is no diffraction. All of the light is reflected (as from a mirror surface) back through the object lens to the photo diode as "light" (or "bright") information. Hence, information recorded on the disc in this pit format is changed to light and dark information which is then converted into an electric signal (called the EFM signal) by the photo diode.

The following description of the focus signals is divided into several steps. The first step describes how the optical system copes when the disc is displaced from the focal point, while the second step describes the

cylindrical lens properties and the focus signal.
Fig.4(1) shows the disc exactly at the focal point, 4(2) shows the change occurring when the disc comes closer to the lens, and 4(3) shows when the disc moves away. In (2) and (3) the forward path from the laser diode has been eliminated to simplify the diagram. And since the grating and concave lens have no direct bearing on the focus signal, these components have also been exluded from the diagram.
In 4(1), the light radiated from the laser diode starts from point O_1, and after being reflected/diffracted at the disc surface, it is brought to a focus at point O_2. As long as the beam remains "in focus" on the disc surface, there will be no change at point O_2. In 4(2) where the disc has come closer to the object lens, the beam is reflected at the disc surface before the focal point is reached, resulting in the reflected beam converging at a point O_3 beyond point O_2. In 4(3) conversely, the beam converges at a point O_4 in front of O_2. In other words, the fact that the beam has been focussed on the disc surface or not can be detected by determining whether the reflected light converges at point O_2 or not.
Fig.5 is a diagramatical outline of the characteristics of the cylindrical lens. In this case, lens action is

vertical, not horizontal. The beam shape is shown at each point (1) thru (7), the beam changing from a straight line at positions (2) and (6) to a circle at position (4). Position (6) corresponds to point O_2 in Fig.4. The photo diode is adjusted to position (4), that is, to form a circle. When the disc is too close to the lens as indicated in Fig.4(2), the beam shape shown in Fig.5 is changed to a straight line at (6) and to an ellipse at (7). That is, the overall shift is towards the shapes shown on the left. As a result, the beam shape at the position of the photo diode is changed from the circle (4) to the lateral ellipse (3). When the disc moves away from the disc as shown in Fig.4(3) with point O_4 being positioned in front of point O_2, on the other hand, the position of the straight line at (6) is displaced towards (5). The shape at the photo diode position, therefore, is changed from a circle (4) to a vertical ellipse (5). These changes at the photo diode position are indicated in Fig.4. And by executing $(B_1 + B_3) - (B_2 + B_4)$ arithmetic operations, the direction of displacement of the focus can be determined from the size of the result of the above operation. As can be seen from the diagram, a result of 0 indicates that the beam is exactly in focus.
In the actual optical path, the cylindrical lens is

rotated through 45° to prevent noise from being included in the focus signal. The photo diode, therefore, apears to be turned through 45° from a ⊘ to a ⊕. Since disc movement towards and away from the lens results in the signal describing an "S" along the horizontal axis if there is no focus servo applied (see Fig.6), this signal is referred to as the S-shaped signal.

The signal used to ensure that the spot of light traces the required track is called the tracking signal. This signal is described on the basis of the outline shown in Fig.7. Light from the laser diode is divided into three portions by the grating. The two side beams (±1 order) on both sides of the center beam are used for the tracking signal. These beams converge (after passing through the optical system) as very small spots on the disc signal surface as indicated in the top of Fig.7. Then after being reflected/diffracted at the signal surface, these beams appear as the respective spots in the plane of the photo diode array as indicated in the bottom of Fig.7. Although the ±1 order beams are drawn very close to the 0 order beam in the top of Fig.7, they are actually about three times further away in the lateral direction.
As can be seen from the diagram, the tracking spots are

adjusted to positions which are displaced towards either side of the relevant track on the disc signal surface. When the A and C outputs are equal (that is, A - C = 0), the ±1 order beams overlap the track by the same degree, and the 0 order beam (which is the beam used to obtain focus error and EFM signals) is exactly over the pits. The relationship between track and the A, B, and C detector outputs is outlined in Fig.8. The bottom diagram depicts a cross-section when the tracks are perpendicular to the page. The A and C outputs at each position are shown in the top diagram. Although the phases of A and C are displaced by 180° as can be seen in the diagram, this can be correctly adjusted by rotating the ±1 order beams in respect to the 0 order beam by grating adjustment. The signal in the middle diagram is obtained by taking the difference between the two signals in the upper diagram, while the bottom diagram shows EFM signal level. When the beam is exactly on the track, A - C = 0, and the EFM signal is at maximum size (best condition).

As can be seen from this description of the optical system, the various optical components each have an important role to play. And the methods employed in pick-up adjustments represent a well balanced and matched

system in terms of overall evaluation of factors such as optical system aberration and disc variations, these methods being selected on the basis of many years of experience in laser disc manufacturing.

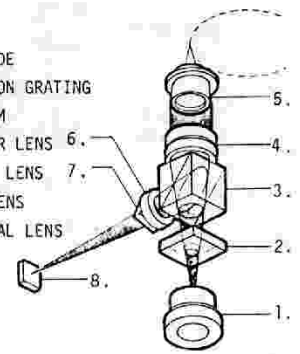


Fig.1 Optical Path and Optical Components

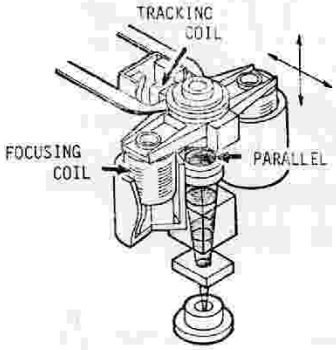


Fig.2 Parallel Rays

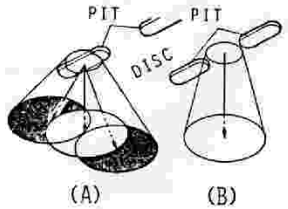


Fig.3 Light Reflected at disc surface

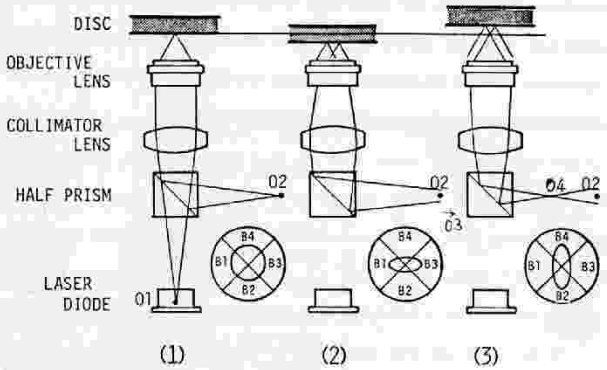


Fig.4 Focal Point Displacement

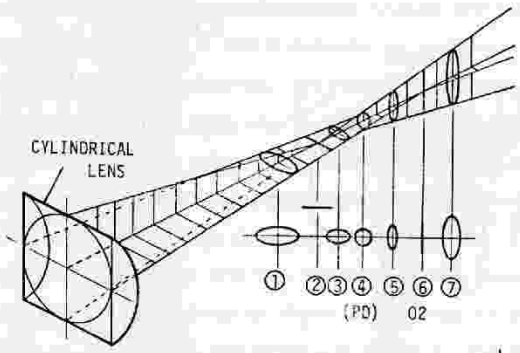


Fig.5 Cylindrical Lens Properties

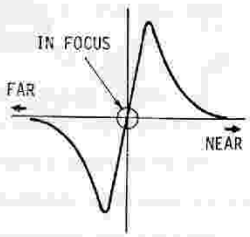


Fig.6 S-Shaped Curve

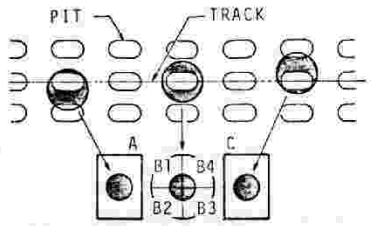


Fig.7 Tracking Error Detection

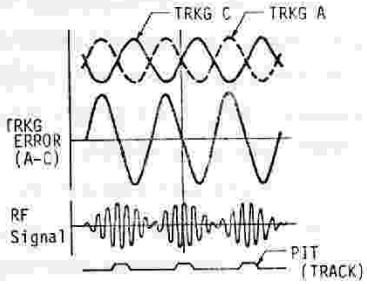


Fig.8 TRKG Error and RF Signal

CONTROL SYSTEM OPERATION

(1) When Power is Switched On

When the power is switched on, $\overline{MUTE}$ is switched on while $\overline{ATT}$ and the focus, tracking, and spindle servos remain off. After these ports have been initialized, the KDCB microcomputers PD4038 and PD4042 are reset and started by $\overline{RESET}$ (pin 26 of PD3007).

If the slider is not in the home position at this time, FWD/REV is set to "L", SCAN to "H", and SLOW/$\overline{FAST}$ to "L". The slider is thus returned towards the center until $\overline{INSIDE}$ becomes "L". If, however, after the slider is stopped at this point as a result of SCAN becoming "L" and SLOW/$\overline{FAST}$ "H", sudden shock displaces the slider from the home position ($\overline{INSIDE}$ "H"), the above homing operation is repeated.

(2) Open/Close Operations

Operations intiated by the OPEN/CLOSE key differ according to the current operating mode and the status of $\overline{CMP}$ and $\overline{DOOR}$.

(a) When the OPEN/CLOSE key is pressed after the power is switched on, or after the STOP key is pressed to stop playback mode

(1) $\overline{CMP}$ = "L" and $\overline{DOOR}$ = "H" --- Port C3 is set to "L" and C4 to "H" to move the disc table out. When the table is moved out as far as it will go and the microswitch is pressed (resulting in $\overline{DOOR}$ being set to "L") ports C3 and C4 both become "L" and the table is stopped. If $\overline{DOOR}$ fails to become "L" within seven seconds (by table movement being held in check by hand) the loading motor is stopped with the table left in that position.

(2) $\overline{CMP}$ = "H" and $\overline{DOOR}$ = "L" --- Port C3 is set to "H" and C4 to "L" to move the table back in. When the table is moved right in and the disc clamped into position (that is, when CMP is set to "L") ports C3 and C4 both become "L" and the table is stopped. Then after being started again for TOC reading, the table is finally stopped. If, however, the table is held in check midway by hand, the circuit which halts motor drive is activated, resulting in the table being stopped in that position. If left in that position, the disc table will be moved out automatically seven

seconds after the OPEN/CLOSE key is pressed.

(3) $\overline{CUP}$ = "H" and $\overline{DOOR}$ = "H" ---- Same operation as described in (2) above.

(b) When the OPEN/CLOSE key is pressed during play, search, or pause mode, the servo mechanisms are switched off, and the slider is returned to the home position. About two seconds after the key is pressed, the eject operation is commenced and the disc table is moved out.

(c) If the OPEN/CLOSE key is pressed during eject or loading operations, ports C3 and C4 are set to "L" and the disc table is stopped. The current operation is then reversed after a 100msec delay.

(3) Set-Up

Set-up mode is initiated when the PLAY or OPEN/CLOSE key is pressed for loading purposes, or when the PLAY key is pressed when the table is stopped after a disc has been loaded. The sequence up to the end of TOC reading is described below.

(1) The slider is returned to the home position if not already in that position. (FWD/$\overline{REV}$ = "L", SCAN = "H", SLOW/$\overline{FAST}$ = "L")

(2) The slider is moved to the outer track and stopped

when $\overline{INSIDE}$ becomes "H".

(3) FOCUS (& LD) is switched on. ($\overline{FOCUS}$ = "L")

(4) The spindle is switched on ($\overline{SPDLRUN}$ = "L") once focus has been locked ($\overline{INFOCUS}$ = "L"). If focus is not locked within 3.5 seconds after being switched on, eject operation is commenced if set-up mode was initiated by the PLAY key, while stop mode is activated if set-up mode was initiated by the OPEN/CLOSE key. If playback mode is about to be started without a disc being loaded, the above eject operation shows the operator that no disc has been loaded. And since the operator may sometimes wish to stop the CD player, stop mode is activated without ejecting when the disc table is moved back in by the OPEN/CLOSE key.

(5) If RF is detected after the spindle is switched on (that is, if $\overline{RF}$ becomes "L"), tracking is closed (TRKG = "L"). If RF is not detected within 600msec after the spindle is switched on, the focus and spindle servos are switched off and operation is stopped. If, for example, a mirror-surface backed disc is loaded with the wrong side up by mistake, operation is stopped because no RF is detected (although nothing wrong is detected by

the focus lock check described in (4) above).

(6) After the tracking has been closed, $\overline{\text{FSLOCK}}$ is monitored by microcomputer. If $\overline{\text{FSLOCK}}$ remains at "L" for 30 consecutive frames (about 4msec) the spindle is judged to be locked, and TOC reading is commenced. If, however, $\overline{\text{FSLOCK}}$ does not remain at "L" for 30 consecutive frames within 3.5 seconds after the tracking is closed, focus, spindle, and tracking are all switched off and operation is stopped.

(7) TOC reading --- The TOC (Table Of Contents) contains (1) the tune number of the first tune on the disc, (2) the tune number of the last tune, (3) the starting time of each tune (in minutes, seconds, and frames from the beginning of the program area), and (4) the read-out start time. Setting up is completed as soon as all of this data is read. Operation is then stopped, or switched to search for the first tune on the disc or the tune of the first step of the program. But since the microprocessor memory capacity is limited, the TOC storage memory can only hold up to 20 tunes. Since CD specifications permit up to 99 tunes to be recorded, TOC reading is completed

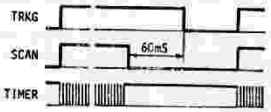
after storing data for the first 20 tunes if a disc containing 21 or more tunes is loaded.
If TOC reading cannot be completed within seven seconds, the reading operation is terminated, followed by a switch to search operation, or stopping of operation.
As long as the disc is not ejected nor the power turned off, the read TOC data is preserved. When operation is next started, search is commenced as soon as the check described in (6) above is successfully completed.

(4) Search

The search sequence is divided into the following five steps.

(a) This operation involves roughly calculating the number of tracks from the difference between the current address and the target address to be sought, setting TRKG to "H", SCAN to "H", and SLOW/$\overline{\text{FAST}}$ to "L", and moving the slider in the FWD or REV direction. Every time the slider moves across a track, a pulse input is applied to the timer terminal (pin 8) of PD3007, the input being counted by the microcomputer. The slider stops when crossing the last of the number

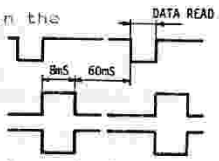
of tracks estimated by the above rough calculation, and TRKG is set to "L" 60msec later. Addresses are then read, and if the target address is reached within one minute, operation proceeds to the next step of the sequence. If the target address is not located, however, the number of tracks is again calculated and slider movement is repeated. The number of tracks is calculated to sufficient accuracy to enable this step to be executed only once or twice before proceeding to the next step.



Since this search method based on calculating the number of tracks utilizes TOC data, this method cannot be used if the TOC cannot be read, or if the TOC can be read but an index search is made. In this case, the number of tracks is fixed to 640 and the above search is repeated until the target address is exceeded. In other words, the target address is approached by repeated opening/closing steps with the width of each slider movement at 640 x 1.6 μm = 1mm (approx.).

(b) After completing the track count search described in (a) the current address (CADR) is compared with the

search address (SADR), and if the CADR $\leq$ SADR condition is met, operation proceeds to the next SLOW FWD step (c). CADR > SADR results in SLOW REV operation. The time chart is outlined in the following diagram.



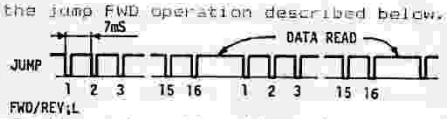
The reason for the 60msec delay between the end of a scanning step and closing of a tracking step is to ensure that the tracking is closed after the actuator (which vibrates radially) has been stabilized after the scanning step.

If the $0 \leq$ CADR - SADR $\leq$ 15 sec. condition is satisfied by repeated SLOW REV operation, the multi-jump reverse operation described in step (d) is activated. If the $0 \leq$ CADR - SADR $\leq$ 15 sec. range is exceeded, however, the following (c) SLOW FWD operation is activated after CADR < SADR is reached.

(c) Apart from FWD/$\overline{\text{REV}}$ being at "H" level, the SLOW FWD time chart is the same as the chart given in (b) above. If the CADR $\geq$ SADR condition is reached, SLOW FWD is stopped and the multi-jump reverse operation described below is activated.

(d) The multi-jump operation involves repeated execution

of 16 jump reverse operations and address comparisons every 7msec until CADR < SADR is attained. This is followed by the jump FWD operation described below.



(e) Jump FWD operations where the address is read and compared with the target address after each forward jump, is repeated until the CADR ≥ SADR condition is met. Once this condition is reached, four or five reverse jumps are made to go back a little (to avoid starting after the actual beginning), and the target address is then approached in playback mode.

In normal search operations, the target address is located by following the steps described above - (a) track count search, (b) slow reverse, (c) slow forward, (d) multi-jump reverse, and (e) jump forward. In the search for the first tune after set-up, however, the search operation commences from step (c) slow forward, step (a) being omitted. A typical search sequence is outlined in Fig.1.

The occurrence of a number of special situations is conceivable during search operations. If the slider jumps out beyond the lead-out during a search, there

is no more RF and $\overline{RF}$ is switched to "H". During search operations, $\overline{RF}$ is checked every 3msec approximately, and if it becomes "H", the tracking is opened with focus and spindle remaining unchanged, resulting in the slider being moved back towards the center (FWD/$\overline{REV}$ = "L", SCAN = "H", and SLOW/$\overline{FAST}$ = "L"). RF is checked during this slider return action, and if RF becomes "L" again, the slider is stopped immediately and tracking is closed. The address is then read, and the search is resumed from the slow forward or slow reverse step. The reason for not restarting from the track count search step is the possibility of forming an endless loop (FWD → $\overline{RF}$ = "H" → $\overline{REV}$ → RF = "L") when searching near the outermost track. If the slider returns all the way to the home position after $\overline{RF}$ becomes "H", operation is switched to stop mode. If a strong shock during the search operation results in a loss of focus, $\overline{SPDLRUN}$ is set to "H" and the spindle stopped to prevent spindle runaway. In this case, too, the slider is returned towards the center. The search is resumed from the slow reverse or slow forward step once the focus is locked again. And if the slider is returned all the way to the home position without regaining proper focus, operation is

again switched to stop mode.
Conversely, when searching for the first tune from the outer track, the slider may sometimes return right back to the home position (where $\overline{\text{INSIDE}}$ becomes "L") during the track count search stage, or it may enter the lead-in zone without quite reaching the home position. If this happens, the slider is stopped and tracking is closed. The address is then read, and the search operation is resumed from the slow forward step. If the slider enters the lead-in zone, track count search is no longer possible since the time difference up to the target address is not known. The search operation, therefore, is resumed from the slow forward step.

(5) Play

After the search for a particular address has been completed, or after pause mode has been released, the muting is switched off and playback mode is commenced. During playback mode, microcomputer control covers (1) monitoring of spindle speed to ensure against runaway action, and (2) switching muting on and off when jumping is caused by shock etc, or when there is a large scratch on the disc surface.

During playback mode, the control microcomputer checks $\overline{\text{RF}}$, $\overline{\text{INFOCUS}}$, and $\overline{\text{FSLOCK}}$ every 13.3msec (98 frames). If a strong shock is received during playback resulting in loss of focus, or if the slider jumps over to the mirror surface, at least one of $\overline{\text{RF}}$, $\overline{\text{INFOCUS}}$, and $\overline{\text{FSLOCK}}$ is switched to "H". Since $\overline{\text{FOCUSON}}$ and $\overline{\text{SPDLRUN}}$ remain at "L" when this happens, an out of focus situation can be returned to focus locked and playback mode. When, however, refocussing is not possible, or when the slider has jumped onto the mirror surface where spindle runaway is about to commence, refocussing or spindle recovery is judged to be impossible if any one of $\overline{\text{RF}}$, $\overline{\text{INFOCUS}}$, and $\overline{\text{FSLOCK}}$ remains at "H" level continuously for 3.5 seconds. Subsequent playback is suspended and operation is stopped.

Muting on/off switching during playback involves checking $\overline{\text{FSLOCK}}$. Although $\overline{\text{RF}}$ and $\overline{\text{INFOCUS}}$ are checked once every 13.3msec, $\overline{\text{FSLOCK}}$ is checked 16 times in the same interval. This corresponds to one check about every 130usec. (equivalent approximately to one frame). Muting is switched on if $\overline{\text{FSLOCK}}$ remains at "H" level for 16 consecutive checks, and is switched off if it remains at "L" level for the same number of

checks. The muting port does not operate in any other case.

(6) Pause

When the PAUSE key is pressed during playback mode, the control microcomputer stores the corresponding address as the pause address (PADR). If a search operation is started during pause mode, and the PAUSE key is then pressed while the search is in progress, the address read upon completion of the search is stored as the PADR. Since the FRAME is not stored in memory on this occasion, the address of the actual pause when the PAUSE key is pressed during a particular second is at the beginning of that second, that is, at FRAME ø.

Each time the current address (CADR) is read during pause mode, it is compared with the PADR, and when CADR $\geq$ PADR is reached, there is a single track jump reverse operation. If shock or vibration results in track jumping back towards the center during pause mode, PADR is reached at the same speed as in playback mode. If the slider jumps outwards, on the other hand, jump reverse is executed continuously until the

CADR < PADR condition is reached. $\overline{RF}$, $\overline{INFOCUS}$, and $\overline{FSLOCK}$ are checked during pause mode in the same way as in playback mode.

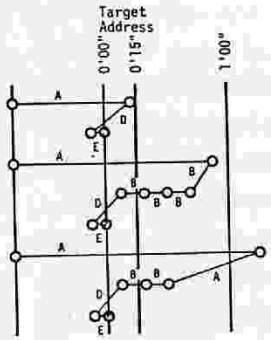
(7) Slow Scanning

Slow scanning is executed by repeated play and jump operations. Since the time taken to jump one track at the innermost track is 120msec, and the corresponding time taken at the outermost track is about 290msec, the playback periods are increased stepwise to ensure that the slow scanning speed remains much the same at the inner and outer tracks. The number of jumps in the FWD direction is 2, and the number of jumps in the REV direction is 4, irrespective of the position on the disc.

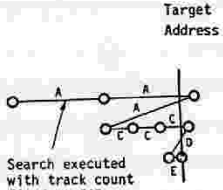
For example, if SLOW SCAN FORWARD is pressed at the inside track, $\overline{ATT}$ is set to "L", and after about 60msec of playback, the slide jumps forward two tracks. This is followed by another 60msec of playback and a two-track jump forward. This cycle is repeated until the outer track is reached where the playback time is about 140msec As soon as the SLOW SCAN key is released, ATT returns to "H", and operation returns to playback or pause mode. If the

lead-out or the lead-in track is reached by slow scan forward or slow scan reverse, the slow scanning operation is stopped and the mode switched to pause, even if the slow scan key is not released.

NORMAL SEARCH

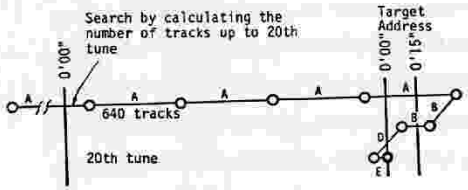


INDEX SEARCH



A. TRACK COUNT SEARCH
B. SLOW REVERSE
C. SLOW FORWARD
D. MULTI JUMP REVERSE
E. JUMP FORWARD

When searching for tunes after the 20th tune



LASER-DIODE HANDLING

Laser diodes are liable to be damaged by electrostatic. Follow the instructions when operating them.

a). Ground the repair bench to the ground line of the power source.

b). Ground your body to the bench.

c). Avoid using equipment which generates high frequency surge or EMI.